64000

HP64000
Logic Development System

Model 64191A
6805 Emulator Controller

HEWLETT
PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

HEWLETT-PACKARD

SERVICE MANUAL

MODEL 64191A

6805 EMULATOR CONTROLLER

REPAIR NUMBERS

This manual applies directly to models with repair numbers prefixed 2301A.

Manual Part Number: 64191-90901
Microfiche Part Number: 64191-90801

PRINTED: JANUARY 1983

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual supports board-level servicing of the Model 64191A 6805 Emulator Controller. It contains installation, parts list, component locator, and schematics for the model 64191A. Operating instructions are provided in a separate operating manual supplied with the instrument. Because the controller only runs with an emulator pod attached, performance test information is included in the service manual for the emulator pod.

1-3. Described in this section are instruments covered, the general features of the emulator controller, power supply loads, and its use with the Hewlett-Packard emulator pods. Also included are conventions used in the manual.

1-4. Shown on the title page is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

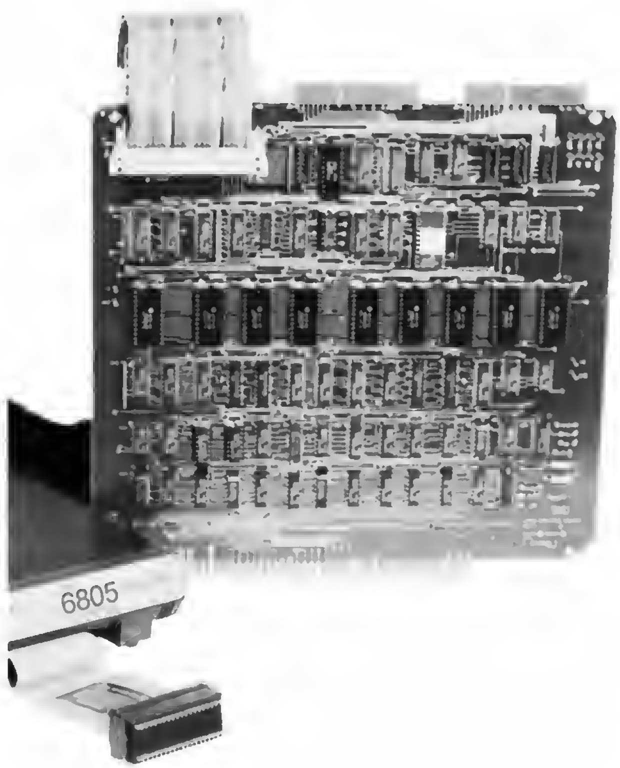


Figure 1-1. 6805 Emulator Controller

1-5. RELATED SERVICE MANUALS.

1-6. Table 1-1 shows the topics covered in the emulator controller and emulator pod service manuals. Service manuals for the models listed below provide additional information.

a. Development station models 64100A and 64110A.

b. Internal analyzer models 64300A and 64302A.

Table 1-1. Emulator Subsystem Service Manuals

Subject	Model 64191A Emulator Controller Service Manual	Emulator Pod Service Manual
General information	yes	yes
Installation	yes	yes
Operation	no, see op manual	no, see op manual
Testing	no, see pod	yes, control & pod
Adjustments	no, none required	no, none required
Parts list	yes, control only	yes, pod only
Service schematics and theory	yes, control only	yes, pod only

1-7. INSTRUMENTS COVERED BY THIS MANUAL.

1-8. Attached to the Model 64191A 6805 Emulator Controller is a repair number tag. The repair number is in the form 0000A00000. It is in two parts; the first four digits and the letter are the prefix and the last five are the suffix. The prefix is the same for each identical model 64191A; it only changes when a change is made to the instrument. The suffix is assigned sequentially and is different for each model 64191A manufactured. This manual applies to each model 64191A with a repair prefix listed on the title page.

1-9. A model 64191A manufactured after the printing of this manual may have a repair number not listed on the title page. The manual for the newer boards is accompanied by a yellow manual change supplement. The supplement explains how to adapt the manual to the newer emulator controller.

1-10. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest manual changes supplement. The supplement is identified by the manual print and part number, both of which appear on the manual title page. Copies are available at the Hewlett-Packard sales/service offices listed in the back of this manual.

1-11. DESCRIPTION.

1-12. Emulation of MC6805 microcomputers is provided by an emulation subsystem consisting of a Model 64191A 6805 Emulator Controller (figure 1-1), an emulator pod, and emulator software. The Model 64191A 6805 Emulator Controller plugs into Hewlett-Packard 64000 system development stations and provides the interface functions between the station, emulator pod, and software analysis options.

1-13. The products in the MC6805 family are single-chip microcomputers with their architecture optimized for controller applications. They have a microprocessor similar to the 6800, a clock oscillator, timer, ROM, RAM, or EPROM, and I/O control, all located on the integrated circuit package. The microcomputers communicate with the outside world through eight bit ports and have various user-specified options that can be hardware masked during manufacture.

1-14. The Model 64191A 6805 Emulator Controller has several important features. The controller contains memory that duplicates the on-chip memory of the 6805 microcomputer being emulated; no additional memory options are needed. This is called foreground memory and is available to the user to load programs and store data. Also located on the controller is background memory, which contains routines that force the emulator processor to perform utility functions.

1-15. The controller hardware passes the identifcation code of the attached emulator pod to the development station so that the appropriate emulator software is used for the menu-driven user interface. This function is particularly important because of the wide variety of options available on the 6805 microcomputer family. When the user enters the desired microcomputer configuration, the controller latches the pod option bits and passes them to the attached emulator pod.

1-16. Based upon the 6805 microcomputer version chosen for emulation, the controller maps foreground memory as ROM and RAM and monitors each access by the emulator processor to see if it is legal. The controller also contains all the control circuitry required to coordinate memory accesses between the development station and the emulator pod.

1-17. Another feature located on the controller is the opcode monitor. This circuitry checks each emulator opcode. When an invalid opcode is found, a break bit can be set.

1-18. All emulator address, data, and status information is tapped on the controller and routed to the emulation bus edge connectors. This bus can be connected to an internal analyzer option card.

1-19. ACCESSORIES SUPPLIED.

1-20. No accessories are supplied with the Model 64191A 6805 Emulator Controller.

1-21. ADDITIONAL EQUIPMENT REQUIRED.

1-22. To operate, the Model 64191A 6805 Emulator Controller must be plugged into a Hewlett-Packard 64000 series development station and connected to an emulator pod for MC6805 series microcomputers.

1-23. POWER REQUIREMENTS.

1-24. Power requirements of the 6805 emulator controller are shown in the table below. Typical power useage is 6 watts.

Table 1-2. Power Supply Loads

Supply	+5 V
Controller current	1.2 A

1-25. CONVENTIONS.

1-26. The following conventions are used in the text and schematics.

a. Abbreviations, see table 6-1.

b. Mnemonics (signal names), see table 8-2.

c. Logic symbols, see table 8-3.

d. Component designators are assigned according to the numbered-row, lettered-column method for integrated circuit packages. Discrete components are assigned reference designators using the upper left to lower right method.

e. TTL logic levels (in volts):

Input high threshold	Input low threshold	Output high threshold	Output low threshold
+2.0	+0.8	+2.4	+0.2

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information necessary to install the Model 64191A 6805 Emulator Controller in the 64000 system. Also included is information concerning initial inspection, damage claims, environmental considerations, storage and shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents have been checked for completeness and the model 64191A has been checked mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the 64191A does not pass performance verification, notify the nearest Hewlett-Packard office. If the shipping container or cushioning material is damaged, notify the carrier as well as the Hewlett- Packard office. Keep the shipping materials for carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. DEVELOPMENT STATION CONFIGURATION.

2-6. The controller should be installed in the highest numbered slot of the development station. When a logic analyzer option card is used with the emulator, the analyzer should be installed in the next lower numbered slot adjacent to the emulator control board. See figure 2-1.

```
     To Pod
       |
       |
  [ Emulator Control ]. . . .highest slot number
  [ Logic Analyzer   ]
  [ Other Options... ]
```

Figure 2-1. Development Station Card Cage

WARNING

Before installing the emulator subsystem, read the safety summary at the front of the manual.

CAUTION

The following precautions should be taken while using Hewlett-Packard emulator pods. Damage to the emulator circuitry may result if these precautions are not observed.

⚠ TURN OFF THE POWER. Turn off power to the user target system and the emulation development station, before inserting the user plug, to avoid circuit damage resulting from voltage transients or mis-insertion of the user plug.

⚠ VERIFY USER PLUG ORIENTATION. Make certain that pin 1 of the target system microprocessor socket, and pin 1 of the user plug, are properly aligned before inserting the user plug into the socket. Failure to do so may result in damage to the emulator circuitry.

⚠ PROTECT AGAINST STATIC DISCHARGE. The emulator pod contains devices which are susceptible to damage by static discharge. Therefore, operators should take precautionary measures before handling the user plug to avoid emulator damage.

⚠ CONNECT THE RFI GROUND BRACKET. The emulator controller and pod can be damaged by static discharge when the emulator pod cable is not firmly clamped in place.

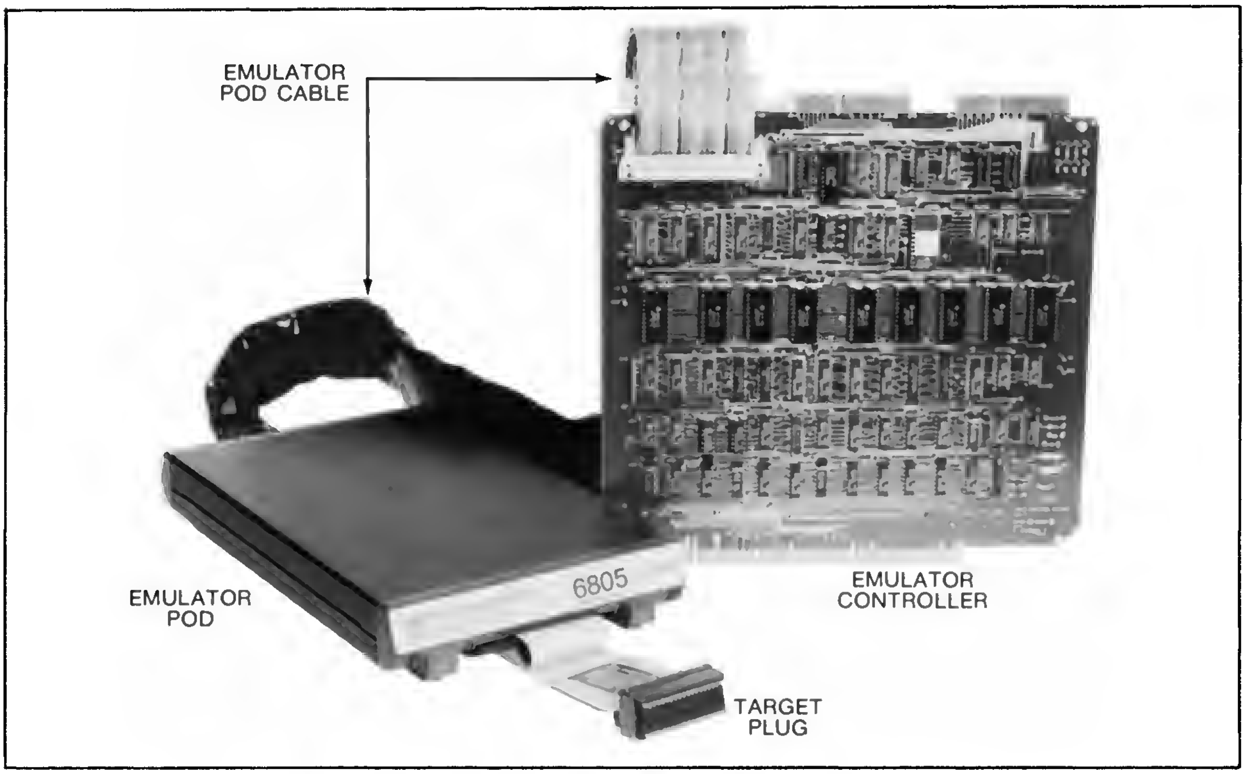


Figure 2-2. Typical 6805 Emulator Subsystem

2-7. INSTALLATION.

2-8. To install the emulator controller and pod proceed as follows:

a. Remove the card cage cover. Position the development station so there is clear access to the card cage.

b. Before placing the controller into the card cage, connect the emulator pod to it as directed in steps c and d.

c. Locate the two multi-colored ribbon cables within the emulator pod cable. One cable is terminated in a female card-edge connector; the other is terminated in a female socket type connector. Locate pin 1, it is indicated by a triangle molded into the connector.

d. Locate the mating male connectors on the controller. They are at the top left of the board, as you face the component side, and have color dots that match dots on the cables. Pin 1 of the male connectors is etched on the board. Align the connectors and attach the cables to the controller.

e. Next, insert the controller into the highest numbered slot. Insure that it is completely seated in the motherboard.

f. Refer to figure 2-3. If the development station has an RFI ground bracket/clamp bar as shown in the figure, perform the next step. If it does not have an RFI ground bracket/clamp bar, attach the bracket/bar as directed on the following page before going to step 'g'.

g. Loosen the clamp bar and slip the emulator pod cable beneath it, placing the wire mesh is directly beneath the bar. Tighten the clamp bar to hold the cable firmly in place.

h. If a logic analyzer option card is to be connected, refer to the appropriate manual and connect it to the control board now.

i. Carefully fold all cables over the boards so as not to damage them. Replace the card cage cover.

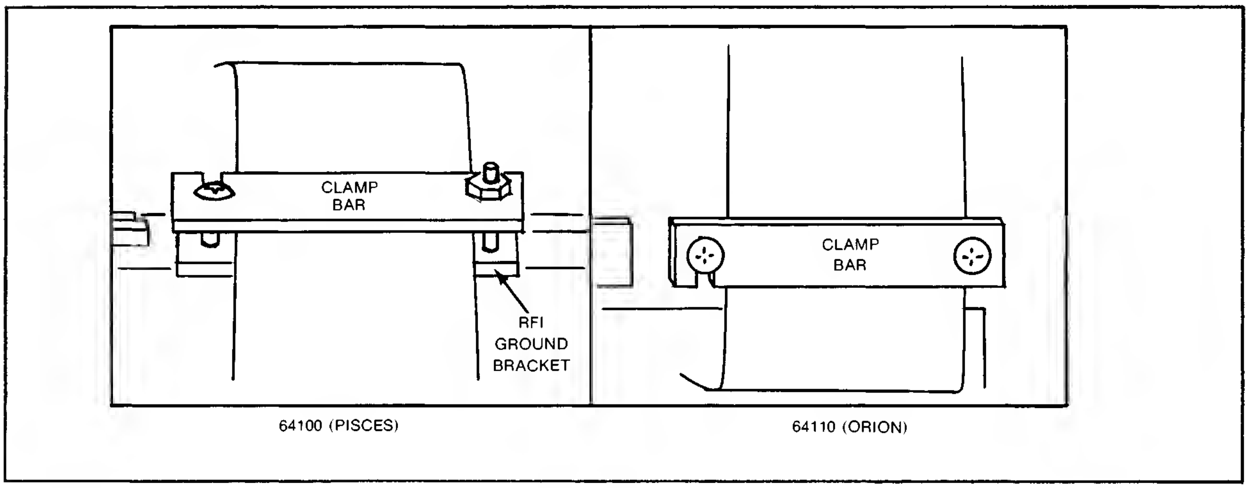


Figure 2-3. RFI Ground Bracket/Clamp Bar

2-9. REMOVAL.

2-10. To remove the controller and pod proceed as follows:

a. Remove the card cage cover. Position the development station so there is clear access to the card cage.

b. If a logic analyzer option card is connected to the controller, disconnect it.

c. Loosen the RFI ground bracket clamp bar and slip the emulator pod cable from beneath it.

d. Next, Remove the controller from the card cage slot.

e. Replace the card cage cover.

2-11. RFI GROUND BRACKET INSTALLATION.

2-12. The emulator pod is shipped with a plastic bag that contains an RFI ground bracket assembly. The assembly includes an RFI ground bracket, clamp bar and miscellaneous hardware. These parts are used in the steps shown below.

2-13. MODEL 64100A DEVELOPMENT STATION.

a. Position the development station so there is clear access to the back.

b. Facing the back, remove the right cable clamp; it is secured by two #6-32 screws along the top edge. Discard these screws.

c. Replace the old cable clamp with the RFI ground bracket, and attach with two new #6-32 x .375 long pan head screws, through the back of the card cage.

d. Locate the clamp bar and position it with the oblong hole over the threaded stud.

e. Install the #6-32 hex nut on the threaded stud, and install the #6-32 x 1.000 long pan head screw in the threaded hole along the top edge of the card cage.

2-14. MODEL 64110A DEVELOPMENT STATION.

a. Position the development station so there is clear access to the back.

b. Facing the back, remove the right cable clamp bracket; it is secured by two #4-40 screws. Discard these screws.

c. Place a number 4 washer on each #4-40 x .750 pan head screw and insert one screw with washer through the oblong hole in the clamp bar. Then mount the clamp bar with the two #4-40 x .750 long pan head screws where the old cable clamp bracket had been.

2-15. OPERATING ENVIRONMENT.

2-16. The Model 64191A 6805 Emulator Controller can be operated in environments within the limits shown below. It should be protected from temperature extremes which cause condensation within the instrument.

Temperature................0°to +40°degrees Celsius.
Humidity...............5 to 80 % relative humidity.
Altitude.......................4 600 m (15 000 ft).

2-17. STORAGE AND SHIPPING ENVIRONMENT.

2-18. The Model 64191A 6805 Emulator Controller can be stored and shipped in environments within the limits given below.

Temperature..............-40°to +40°degrees Celsius.
Humidity................5 to 80 % relative humidity.
Altitude......................15 240 m (50 000 ft).

2-19. ORIGINAL PACKAGING.

2-20. Containers and packing materials identical to those used in factory packaging are available through Hewlett-Packard sales and service offices.

2-21. OTHER PACKAGING.

2-22. The following general instructions should be used for repackaging with commercially available materials.

a. Wrap the Model 64191A 6805 Emulator Controller in heavy paper or plastic. Use a strong shipping container. A double wall carton made of 350 pound test material is adequate.

b. Use a layer of shock absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the model 64191A to provide firm cushioning and prevent movement inside the container

c. Seal shipping container securely.

d. Mark shipping container FRAGILE to request careful handling.

e. In any correspondence, refer to instrument by model number and full repair number.

SECTION III

OPERATION

The operation of the Model 64191A 6805 Emulator Controller is a function of the HP 64000 system software. Complete operation from the development station keyboard is beyond the scope of this service manual. Please refer to the operator's manuals for the procedures.

SECTION IV

PERFORMANCE TESTS

This service manual does not contain performance test information. To test the Model 64191A 6805 Emulator Controller, it must be connected to a Hewlett-Packard 6805 series emulator pod. Refer to the service manual for the emulator pod being used.

SECTION V

ADJUSTMENTS

There are no adjustments on the Model 64191A 6805 Emulator Controller.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts for the Model 64191A 6805 Emulator Controller. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one, all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS.

6-6. Table 6-2, the replaceable parts list, is organized as follows:

a. Chassis mounted parts in alphanumerical order by reference designator.

b. Electrical assemblies and their components in alphanumerical order by reference designator.

c. Miscellaneous parts.

6-7. The total quantity for each part is given only once, at the first appearance of the part number in the list. The information given for each part consists of the following.

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five digit code that indicates the manufacturer.

e. The manufacturer's part number.

6-8. ORDERING INFORMATION.

6-9. to order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-10. to order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-11. DIRECT MAIL ORDER SYSTEM.

6-12. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP parts center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount, for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-13. Mail order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**O**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

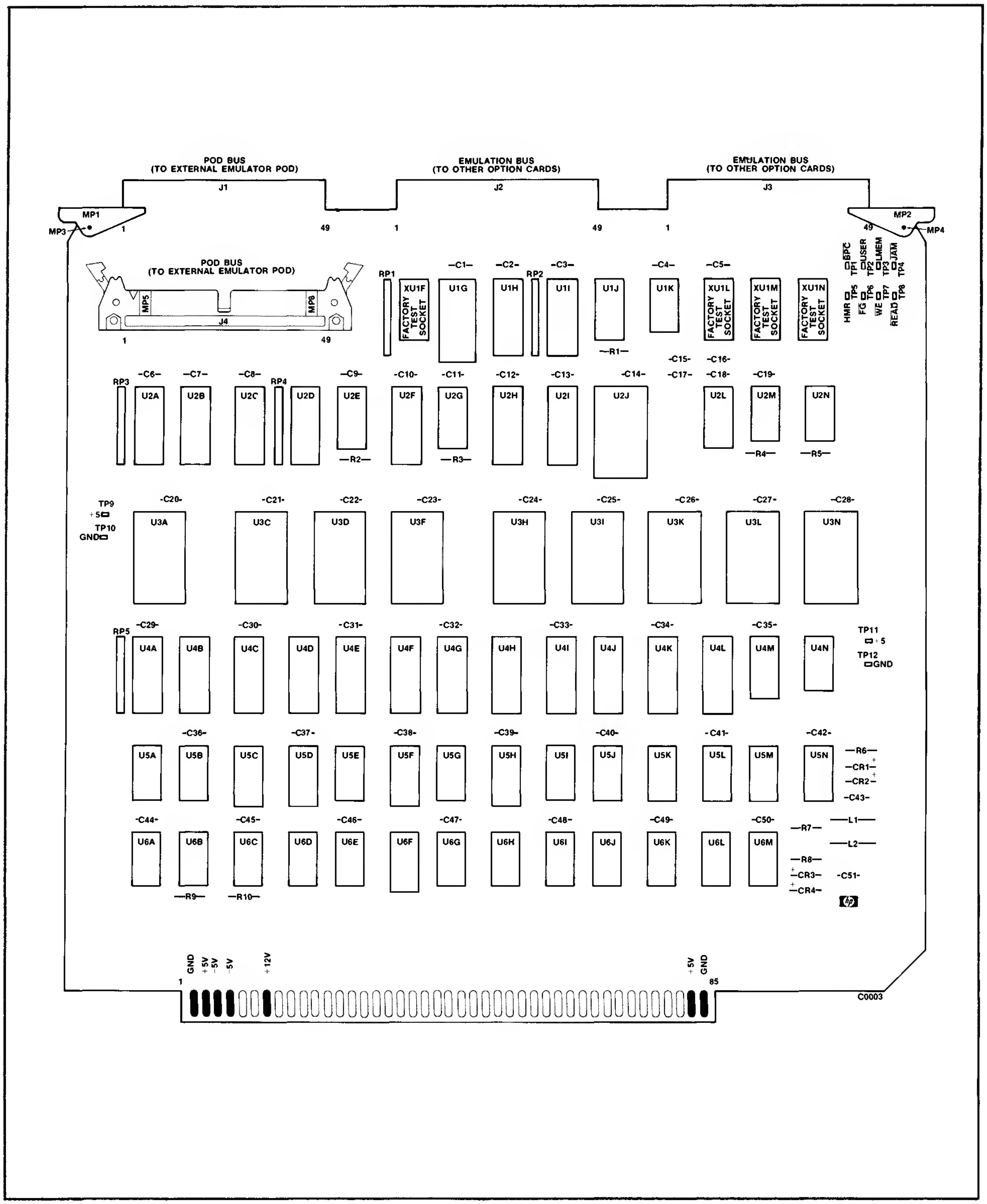


Figure 6-1. Component Locator

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64191A	2	1	6805 EMULATOR CONTROLLER	28480	64191A
A1	64191-66501	4	1	PC BOARD ASSEMBLY-CONTROL	28480	64191-66501
C1	0160-5321	8	48	CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C2	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C3	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C4	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C5	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C6	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C7	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C8	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C9	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C10	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C11	0160-5371	8	1	CAPACITOR-FXD CER 1000PF +/-20	28480	0160-5371
C12	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C13	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C14	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C15	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C16	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C17	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C18	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C19	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C20	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C21	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C22	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C23	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C24	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C25	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C26	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C27	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C28	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C29	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C30	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C31	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C32	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C33	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C34	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C35	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C36	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C37	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C38	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C39	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C40	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C41	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C42	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C43	0160-5507	2	1	CAPACITOR-FXD 390PF	28480	0160-5507
C44	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C45	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C46	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C47	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C48	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C49	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C50	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
C51	0160-5573	2	1	CAPACITOR-FXD 560PF	28480	0160-5573
CR1	1901-0040	1	4	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
J4	1251-5653	3	1	CONNECTOR- 50 POSITION MREJT	28480	1251-5653
L1	9140-0179	1	2	INDUCTOR RF-CH-MLD 22UH 10% .166DX.385LG	28480	9140-0179
L2	9140-0179	1		INDUCTOR RF-CH-MLD 22UH 10% .166DX.385LG	28480	9140-0179
MP1	64191-85001	9	1	BOARD EXTRACTOR - 64191A	28480	64191-85001
MP2	64191-85002	0	1	BOARD EXTRACTOR- FM 6805	28480	64191-85002
MP3	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
MP4	1480-0116	8		PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
MP5	1251-5595	2	2	POLARIZING KEY	28480	1251-5595
MP6	1251-5595	2		POLARIZING KEY	28480	1251-5595
R1	0757-0280	3	7	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R3	0757-0470	3	1	RESISTOR 162K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1623-F
R4	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R6	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R7	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R8	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R9	0757-0407	6	2	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
R10	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
RP1	1810-0430	0	5	NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
RP2	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
RP3	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
RP4	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
RP5	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
TP12	0360-0535	0	12	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1G	1816-1308	5	1	IC-93L422 PC	07263	93L422PC
U1H	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U1I	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U1J	1820-1217	4	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS151N
U1K	1820-1202	7	3	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U2A	1820-1624	7	1	IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U2B	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U2C	1820-1997	7	7	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U2D	1820-1917	1	4	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U2E	1820-1130	0	1	IC GATE TTL S NAND 13-INP	01295	SN74S133N
U2F	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U2G	1820-1423	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
U2H	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U2I	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U2J	64191-80000	8	1	OPCODE MONITOR ROM	28480	64191-80000
U2L	1820-1430	3	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U2M	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U2N	1820-1205	0	1	IC GATE TTL LS AND DUAL 4-INP	01295	SN74LS21N
U3A	1818-1611	7	9	IC-HM6116P-3	S4013	HM6116P-3
U3C	1818-1611	7		IC-HM6116P-3	S4013	HM6116P-3
U3D	1818-1611	7		IC-HM6116P-3	S4013	HM6116P-3
U3F	1818-1611	7		IC-HM6116P-3	S4013	HM6116P-3
U3H	1818-1611	7		IC-HM6116P-3	S4013	HM6116P-3
U3I	1818-1611	7		IC-HM6116P-3	S4013	HM6116P-3
U3K	1818-1611	7		IC-HM6116P-3	S4013	HM6116P-3
U3L	1818-1611	7		IC-HM6116P-3	S4013	HM6116P-3
U3N	1818-1611	7		IC-HM6116P-3	S4013	HM6116P-3
U4A	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U4B	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U4C	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U4D	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U4E	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U4F	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U4G	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U4H	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U4I	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U4J	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U4K	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U4L	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U4M	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U4N	1820-1144	6	5	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U5A	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U5B	1820-1206	1	1	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U5C	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U5D	1820-1282	3	3	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
U5E	1820-1112	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U5F	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U5G	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U5H	1820-1282	3		IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
U5I	1820-1210	7	1	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
U5J	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U5K	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U5L	1820-1197	9	4	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U5M	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U5N	1820-1307	3	1	IC SCHMITT-TRIG TTL S NAND QUAD 2-INP	01295	SN74S132N
U6A	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U6B	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U6C	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U6D	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U6E	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U6F	1820-1282	3		IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
U6G	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U6H	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U6I	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U6J	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U6K	1820-1274	3	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS22N
U6L	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U6M	1820-1285	6	1	IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
XU1F	1200-0607	0	6	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU1G	1200-0612	7	1	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU1L	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU1M	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU1N	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
XU2G	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU2J	1200-0541	1	10	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU3A	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU3C	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU3D	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU3F	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU3H	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU3I	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU3K	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU3L	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU3N	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU5C	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607

Table 6-3. List of Manufacturers' Codes

Mfr. No.	Manufacturer Name	Address		Zip Code
S4013	HITACHI	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304

SECTION VII

MANUAL CHANGES

This section normally contains backdating information for models with repair numbers prior to the one shown on the title page. Because this edition includes only the first repair number, there is no backdating material.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains reference information for servicing the Model 64191A 6805 Emulator Controller. For convenience, the schematics, component locator, and other service information are provided on foldout sheets.

8-3. The purpose of the emulator controller is to act as an interface between the development station, emulator pod, and other option cards. To do this, the controller coordinates status and control bits, manages emulation memory, monitors emulator opcodes, and places emulator address, data, and status on the emulation bus within the development station. The following functional blocks implement these operations.

	Schematic
Development Station Interface..........	1
Control................................	2
Foreground/Background Memory...........	3
Pod Interface and Memory Monitor.......	4
Last Address and Break Logic...........	5
Foreground/Background Logic............	6
Pod Interface and Opcode Monitor.......	7

8-4. GENERAL THEORY.

8-5. Perhaps the most important task of the controller hardware is to manage memory. Therefore, a good way to understand the emulator controller is to examine the functions of foreground and background memory.

8-6. Foreground memory is provided on the controller as a substitute for the on-chip memory of the 6805 microcomputer. When the user selects a version of the 6805 to emulate, software automatically maps foreground memory into 64 byte blocks that correspond to the on-chip memory of the 6805. That is, it is mapped as RAM or ROM. This memory space is available to the user to load programs or store data.

8-7. Each 6805 also has internal registers in the address space between 0 and 15. These addresses cannot be mapped in the foreground memory, but must remain as on-chip addresses. These 16 addresses are called user memory and typically are used for port data and direction control, and on-chip timer functions.

8-8. Background memory is not available to the user. It is loaded with utility routines by the emulator software. Typically, the routines instruct the emulator processor to read its own internal registers and store the information in background so the development station can read it. The emulator processor is forced to run these routines when the opcode for a software interrupt (SWI) is jammed onto its data bus.

8-9. Thus, the emulator processor is either running user programs in foreground memory, or it is running service routines in background memory.

8-10. When the user performs such tasks as loading progams into memory, or modifying a memory location, the development station issues a break to the emulator processor and forces it into background memory. In background, the emulator processor performs a wait loop while the development station processor accesses foreground memory. In this manner, the development station processor has complete access to the memory being used by the emulator.

8-11. It is the function of the emulator hardware to coordinate all the memory related operations described above. In addition, the controller hardware monitors all opcodes used by the emulator processor to see if they are valid. The controller also places all emulator processor address, data, and status information on the emulation bus inside the development station. This bus can be monitored by an attached internal logic analyzer option card. The following paragraphs describe in detail the functional blocks and operation of the controller.

8-12. DEVELOPMENT STATION INTERFACE, SCHEMATIC 1.

8-13. This circuitry includes break, pod option, and pod status registers, plus data and address bus buffering. The circuitry allows the development station to communicate with the controller.

8-14. BREAK, OPTION & STATUS REGISTERS, SCHEMATIC 1.

8-15. Break register U4L latches six bits that control the emulator operation. These bits are written to the controller by the development station. Five of the bits control breaks in operation and one, LEXT, selects a signal source. The bits are,

LDEFIB....initialize operation, set to known state.
LBPCBRK...stop operation at development station request.
LOPCBRK...stop when an illegal opcode is detected.
LMEMBRK...stop when an illegal address is detected.
LROMBRK...stop when an a write to 'ROM' is attempted.
LEXT......select external crystal clock source

8-16. Option register U2C is a latch/driver that receives data from the development station via the LD0-7 data bus. These bits are used to drive the pod option bus LPOPT0-7. The attached emulator pod reads these bits and uses the information to configure pod operation. These bits implement the choices of emulator configuration selected by the user; for example, type of 6805 being emulated, clock source, timer clock source, and timer prescaler value.

8-17. The emulator status register consists of U4K, a buffer/driver, and U4A, a latch/driver. The status bits are,

LNCLK......slow, or no processor clock.
HFG........emulator is executing in foreground memory.
LILLOPC....illegal opcode detected.
LILLMEM....illegal memory operation detected.
LRESET.....target system has requested processor reset.
LIRQ.......target system has requested processor interrupt.
HTIMER.....target system has enabled processor timer to count.
LICE.......emulator plug is in target system, and receiving +5v.

8-18. DEVELOPMENT STATION DATA BUS BUFFER, SCHEMATIC 1.

8-19. Data transfer from the controller to the development station is controlled by chips U4H and U4I. The data-out latch U4H drives the LD0-7 data bus when the development station reads emulation memory. The emulator board identification is placed on the LD0-7 bus by U4I when the development station requests the board ID. Four bits of ID come from the controller and four come from the attached emulator pod.

8-20. Data transfer to the controller from the development station is controlled by chip U4J. Data is received from the development station via the LD0-7 data bus and is buffered onto the LED0-7 data bus.

8-21. DEVELOPMENT STATION ADDRESS BUS BUFFER, SCHEMATIC 1.

8-22. The development station address bus LA0-15 is received by the controller at buffer/drivers U4D and U4E. These chips then drive the controller LEA0-15 address bus.

8-23. CONTROL LOGIC, SCHEMATIC 2.

8-24. The main elements of the control circuitry are the board select, memory access control, register address decoder, and write enable logic. These circuits control access to foreground memory, background memory, and various registers located on the controller. Three main tasks performed by the circuitry are as follows.

8-25. One, the logic arbitrates requests between the attached pod, and the development station. Second, the logic decides if the access is to foreground memory, background memory, or to various registers. Third, the controller implements the read, or write, as requested. The majority of this circuitry is shown on schematic 2. Foreground/background memory circuitry is shown on schematic 3.

8-26. BOARD SELECT LOGIC, SCHEMATIC 2.

8-27. The board select logic determines when the development station wants to access memory. This is done by decoding the LSTM, LSEL, LID, LA12 and LA13 to produce HMR (high memory request). The logic looks at BLMEM (buffered low memory) to determine when the pod is requesting a memory access.

8-28. MEMORY ACCESS CONTROL LOGIC, SCHEMATIC 2.

8-29. The memory access control logic arbitrates between development station and pod access. Queuing flip-flop U5K places competing requests into a queue, so only one request is serviced at a time. When the development station requests a memory access, the read/write logic decodes LA12 and LA13 at NOR gate U6L. When both lines are high, the access is to the various registers, and the register address decoder U5F is enabled. When LA12 is low, the access is to foreground or background memory (see schematic 3). In this case, signal LA13 is decoded by foreground memory gate U5I and background memory gate U4N.

8-30. When the attached emulator pod requests a memory access, the monostable multivibrator U2G generates LMSYN (low memory synch). This signal to the development station causes the station processor to hold off its memory operation until the line goes high, indicating the pod access is complete.

8-31. REGISTER ADDRESS DECODER, SCHEMATIC 2.

8-32. Decoder U5F controls development station access to the registers shown below.

Pod Option Register
Status Register
Break Register
Last Address Register
Last Opcode (address) Register

8-33. WRITE ENABLE LOGIC, SCHEMATIC 2.

8-34. The write enable logic consists of AND-OR gate U6M and discrete linear components in an LRC network. The read enable logic is shown on schematic 3, and consists of AND-OR gate U5I for foreground memory and OR gate U4N for the background memory. The foreground memory RAM chips are selected by decoder U5C which decodes address lines LEA10-13.

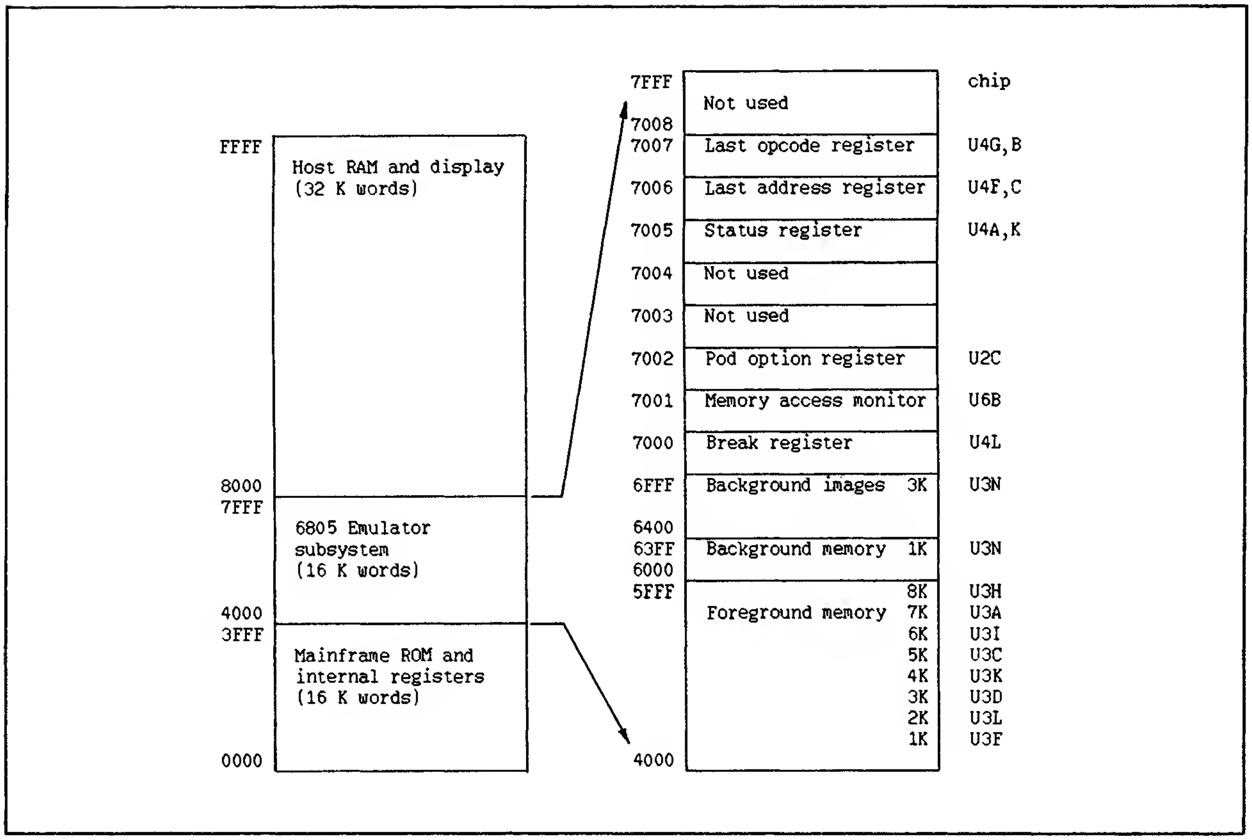


Figure 8-1. Emulator Memory Map

8-35. FOREGROUND/BACKGROUND MEMORY, SCHEMATIC 3.

8-36. The foreground memory consists of eight RAM chips. Each chip is a 2K x 8 bit RAM; however, pin 19 is grounded causing only the lower 1K of memory to be directly accessible. The background memory consists of a single RAM chip configured the same way as foreground memory.

8-37. Gates U5I and U4C decode foreground/background choices. Signal LA13 is decoded by foreground memory gate U5I and background memory gate U4N. Lines LEA10-12 are decoded by U5C to select the appropriate foreground RAM chip.

8-38. POD INTERFACE AND MEMORY MONITOR, SCHEMATIC 4.

8-39. This circuitry includes the pod data bus buffer, data bus jam buffer, pod address bus buffer, memory access monitor RAM, and port address detector. The circuitry allows the controller to transfer data to the attached pod and to monitor the addresses accessed by the pod.

8-40. POD DATA BUS BUFFER, SCHEMATIC 4.

8-41. Data transfers between the controller and attached emulator pod occur over the HD0-7 data bus. The data-in buffer/driver U2H receives the data from the pod and then drives it onto the LED0-7 data bus. Data is output from the controller to the attached pod by buffer/driver U1I.

8-42. DATA BUS JAM BUFFER, SCHEMATIC 4.

8-43. To force the emulator into background memory, buffer/driver U1H 'jams' the SWI opcode (software interrupt) onto the HD0-7 data bus.

8-44. POD ADDRESS BUS BUFFER, SCHEMATIC 4.

8-45. The controller receives addresses from the attached emulator pod. These addresses appear on the HEA0-15 address bus and are received by buffer/drivers U2D and U2E. These chips then drive the LEA0-15 address bus.

8-46. MEMORY ACCESS MONITOR RAM, SCHEMATIC 4.

8-47. RAM U1G monitors the foreground memory addresses accessed by the pod. Its data output lines indicate the type of memory being accessed; see below.

HGUARD.....when high, memory is outside range of 6805 being emulated.

HINT.......when high, memory is above address 63, ie. internal to the controller. When low, address is on-chip, ie. user memory.

HRAM.......when high, memory is mapped as RAM; when low, memory is mapped as ROM.

8-48. The memory access monitor is loaded by a development station write to address 7001H, which clears flip-flop U6B and allows the emulator pod write signal HPODWRT to be gated through U6A to the RAM. The final write to an address less than 0010H sets U6B and disables emulator processor writes to the memory access monitor.

8-49. PORT ADDRESS DETECTOR, SCHEMATIC 4.

8-50. Chip U2E is a NAND gate that monitors the address bus. Whenever an address in the range 0-15 is detected, its output LPORTS goes low. The addresses 0 - 15 are generally port or timer addresses, and are not mapped on the controller foreground memory.

8-51. LAST ADDRESS AND BREAK LOGIC, SCHEMATIC 5.

8-52. This circuitry consists of the last address registers and the break logic. It allows the controller to force breaks in emulator operation and record the last memory address accessed.

8-53. LAST ADDRESS REGISTERS, SCHEMATIC 5.

8-54. There are two registers on the controller that latch the address of a memory access. The last opcode register latches the memory address every time the pod processor reads in an opcode. This is accomplished by using the LOPCREG signal to clock the latches.

8-55. The last address register is clocked every time there is a foreground memory access. Whenever a break occurs, the break logic generates LBREAK which disables the clock inputs to the latches so that the registers cannot be written over. Later, the development station can read these registers to see what the last opcode address and the absolute last address were when the break occurred.

8-56. BREAK LOGIC, SCHEMATIC 5.

8-57. The break logic responds to breaks from the development station, from an attached internal analysis card on the emulation bus, and to breaks caused by illegal operations. The illegal opcode flip-flop U6C sets LBREAK whenever the user has chosen to break when an invalid opcode is detected. The illegal memory flip-flop U6B sets LBREAK when an illegal memory operation is detected. This occurs whenever an access is made to guarded memory. The user cannot override this action. When the user choses to break on a write to memory mapped as ROM there is a break.

8-58. FOREGROUND/BACKGROUND LOGIC, SCHEMATIC 6.

8-59. Flip-flop U5H is the foreground/background controller, and when set, forces the emulator to execute in background memory. It is set by either the LDEFIB signal or the presence of a break. This causes jam flip-flop U6E and gate U6D to produce LJAM, which forces the emulation processor into a software interrupt (SWI opcode). The processor status is pushed onto its stack as the processor enters the background state.

8-60. The emulator is released from the background state by flip-flop U6F when the lastcycle of the opcode occurs and LEA10 goes low, indicating execution of an opcode at an address greater than 0400H. Background memory above 0400H is loaded with the RTI opcode (return to interrupt) and causes the processor to continue operation from the SWI point.

8-61. There are times when the emulator is executing in background that a memory access must be made to the user memory; such as when memory display is requested by the user. To do this, the background routine issues a write to a background address greater than 0400H. Gate U5G detects this by looking at the HREAD (pod), and LEA10 lines. When detected, user memory operation flip- flop U6F is set and the lower four data bits of the write are loaded into user memory operation counter U4M. When the counter reaches terminal count, the HFGMEM signal is enabled for one cycle, allowing the access to user memory. The emulator immediately returns to background after the operation.

8-62. POD INTERFACE AND OPCODE MONITOR, SCHEMATIC 7.

8-63. This circuitry includes control bit buffer/drivers, pod option bus, status bus, pod identification bus, and the opcode monitor logic. It allows operating information to be passed between the pod and controller, for the controller to monitor the opcodes being executed by the emulator processor.

8-64. CONTROL BIT BUFFER/DRIVERS, SCHEMATIC 7.

8-65. Chips U2A and U2B drive and receive several control bits that are transferred between the controller and the attached pod. Each of the signals is explained in the table of mnemonics, table 8-2.

8-66. OPCODE MONITOR LOGIC, SCHEMATIC 7.

8-67. Latch U2I latches each opcode read by the emulator pod. The outputs of the latch directly drive the address lines the 2K x 8 bit opcode monitor ROM U2J. The ROM data lines are always enabled and feed the opcode cycle counter U2L and the opcode status bit selector U1J.

8-68. The ROM data bits indicate if the opcode is a valid or not. This includes checking whether the opcode is valid for the 6805 microcomputer being emulated. Not all opcodes are valid for all versions of the 6805. When the opcode is valid, the ROM data bits also load the cycle counter with the number of machine cycles in the opcode. The counter then counts to terminal count which is the HLASTCYCLE line, which tells the controller the opcode is about to be finished.

8-69. The opcode status bit selector gates the opcode status bit from the opcode ROM through to the emulation bus, where it can be read by an attached software analyzer. The bit, LES2, indicates whether the opcode is a read or write, etc.

8-70. Flip-flop U5E detects when the emulator is in foreground memory and drives an input to AND gate U2M. The gate then generates the LANAL signal when the pod is accessing memory. Signal LANAL tells an attached analyzer that the emulation bus has valid information on it.

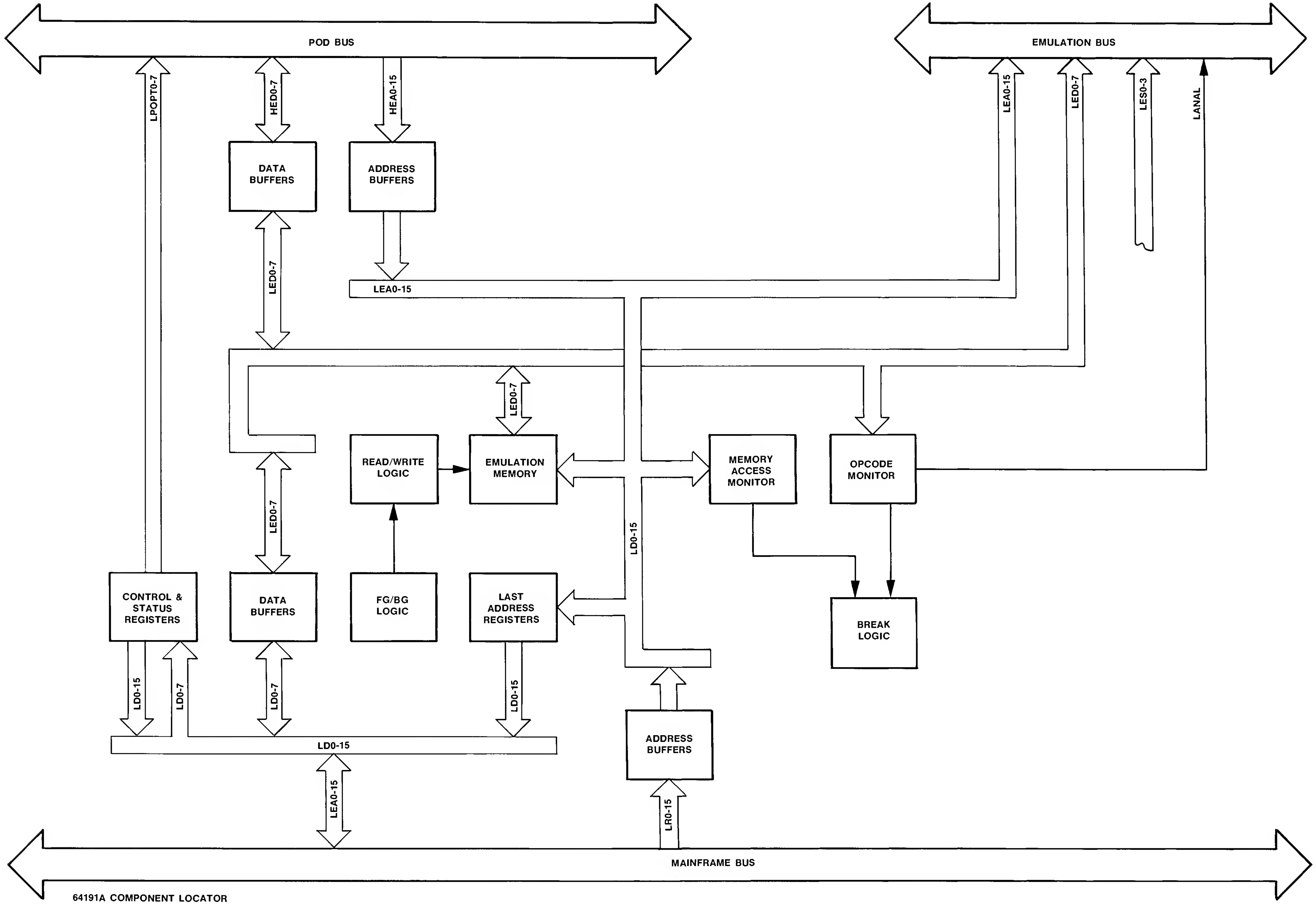


Figure 8-2. Emulator Controller Block Diagram

Table 8-1. Connector Signals

Connector P1, Schematic 1				Connector J1, Schematic 4		Connector J2, Schematic 7		Connector J3, Schematic 4		Connector J4, Schematic 7	
Pin				Pin		Pin		Pin		Pin	
1	gnd	53	SGND	1	HEA15	1	LBRK	1	LEA0	1	LMEM
2	gnd	54	SGND	2	gnd	2	not used	2	gnd	2	gnd
3	+5 v	55	LHSYN	3	HEA14	3	gnd	3	LEA1	3	LREAD
4	+5 v	56	LVSYN	4	gnd	4	gnd	4	gnd	4	gnd
5	-5.2 v	57	LVID	5	HEA13	5	LED0	5	LEA2	5	HOPFETCH
6	-5.2 v	58	LIVIDT	6	gnd	6	LED1	6	gnd	6	gnd
7	-5.2 v	59	SGND	7	HEA12	7	LED2	7	LEA3	7	LEXT
8	-5.2 v	60	SGND	8	gnd	8	LED3	8	gnd	8	+5 v
9	-3.2 v	61	LBYTE	9	HEA11	9	LED4	9	LEA4	9	BLRESET
10	-3.2 v	62	LUPB	10	gnd	10	LED5	10	gnd	10	gnd
11	-12 v	63	LSTM	11	HEA10	11	LED6	11	LEA5	11	LFG
12	-12 v	64	LSTB	12	gnd	12	LED7	12	gnd	12	+5 v
13	+12 v	65	LWRT	13	HEA9	13	gnd	13	LEA6	13	LPORTS
14	+12 v	66	LMSYN	14	gnd	14	gnd	14	gnd	14	gnd
15	+17 v-ret	67	LID	15	HEA8	15	LED8	15	LEA7	15	HUSER
16	+17 v	68	LMAP1	16	gnd	16	LED9	16	gnd	16	+5 v
17	+40 v	69	LMAP2	17	HEA7	17	LED10	17	LEA8	17	HFGMEM
18	not used	70	LMAP3	18	gnd	18	LED11	18	gnd	18	gnd
19	LA0	71	LIR1	19	HEA6	19	LED12	19	LEA9	19	HDEFIB
20	LA1	72	LSEL	20	gnd	20	LED13	20	gnd	20	+5 v
21	LA2	73	BNC4	21	HEA5	21	LED14	21	LEA10	21	LIRQ
22	LA3	74	LOPC	22	gnd	22	LED 15	22	gnd	22	gnd
23	LA4	75	BNC3	23	HEA4	23	gnd	23	LEA11	23	HTIMER
24	LA5	76	LPOP	24	gnd	24	gnd	24	gnd	24	+5 v
25	LA6	77	BNC2	25	HEA3	25	LEBYT	25	LEA12	25	LPSTAT3
26	LA7	78	BNC1	26	gnd	26	gnd	26	gnd	26	gnd
27	LA8	79	SGND	27	HEA2	27	LEBUP	27	LEA13	27	LPSTAT4
28	LA9	80	SGND	28	gnd	28	gnd	28	gnd	28	+5 v
29	LA10	81	25MHz	29	HEA1	29	LREFREQ	29	LEA14	29	LPSTAT5
30	LA11	82	not used	30	gnd	30	gnd	30	gnd	30	gnd
31	LA12	83	+5 v	31	HEA0	31	HREFAK	31	LEA15	31	LPSTAT6
32	LA13	84	+5 v	32	gnd	32	gnd	32	gnd	32	gnd
33	LA14	85	gnd	33	HED7	33	LMBRKS	33	LEA16	33	LICE
34	LA15	86	gnd	34	gnd	34	gnd	34	LEA20	34	gnd
35	SGND			35	HED6	35	LBKG	35	LEA17	35	LPOPT0
36	SGND	To Development		36	gnd	36	gnd	36	LEA21	36	gnd
37	LD0	Station		37	HED5	37	not used	37	LEA18	37	LPOPT1
38	LD1			38	gnd	38	gnd	38	LEA22	38	gnd
39	LD2			39	HED4	39	LANAL	39	LEA19	39	LPOPT2
40	LD3			40	gnd	40	gnd	40	LEA23	40	PID0
41	LD4			41	HED3	41	LES0	41	HMAV	41	LPOPT3
42	LD5			42	gnd	42	LES1	42	gnd	42	PID1
43	LD6			43	HED2	43	LES2	43	HREADY	43	LPOPT4
44	LD7			44	gnd	44	LES3	44	gnd	44	PID2
45	LD8			45	HED1	45	LES4	45	LEWRT	45	LPOPT5
46	LD9			46	gnd	46	LES5	46	gnd	46	PID3
47	LD10			47	HED0	47	LES6	47	LWDV	47	LPOPT6
48	LD11			48	gnd	48	LES7	48	gnd	48	+12 v
49	LD12			49	not used	49	gnd	49	HUSER	49	LPOPT7
50	LD13			50	-5.2 v	50	gnd	50	gnd	50	+12 v
51	LD14										
52	LD15			To Emulator Pod		To Internal Analyzer		To Emulator Pod		To Internal Analyzer	

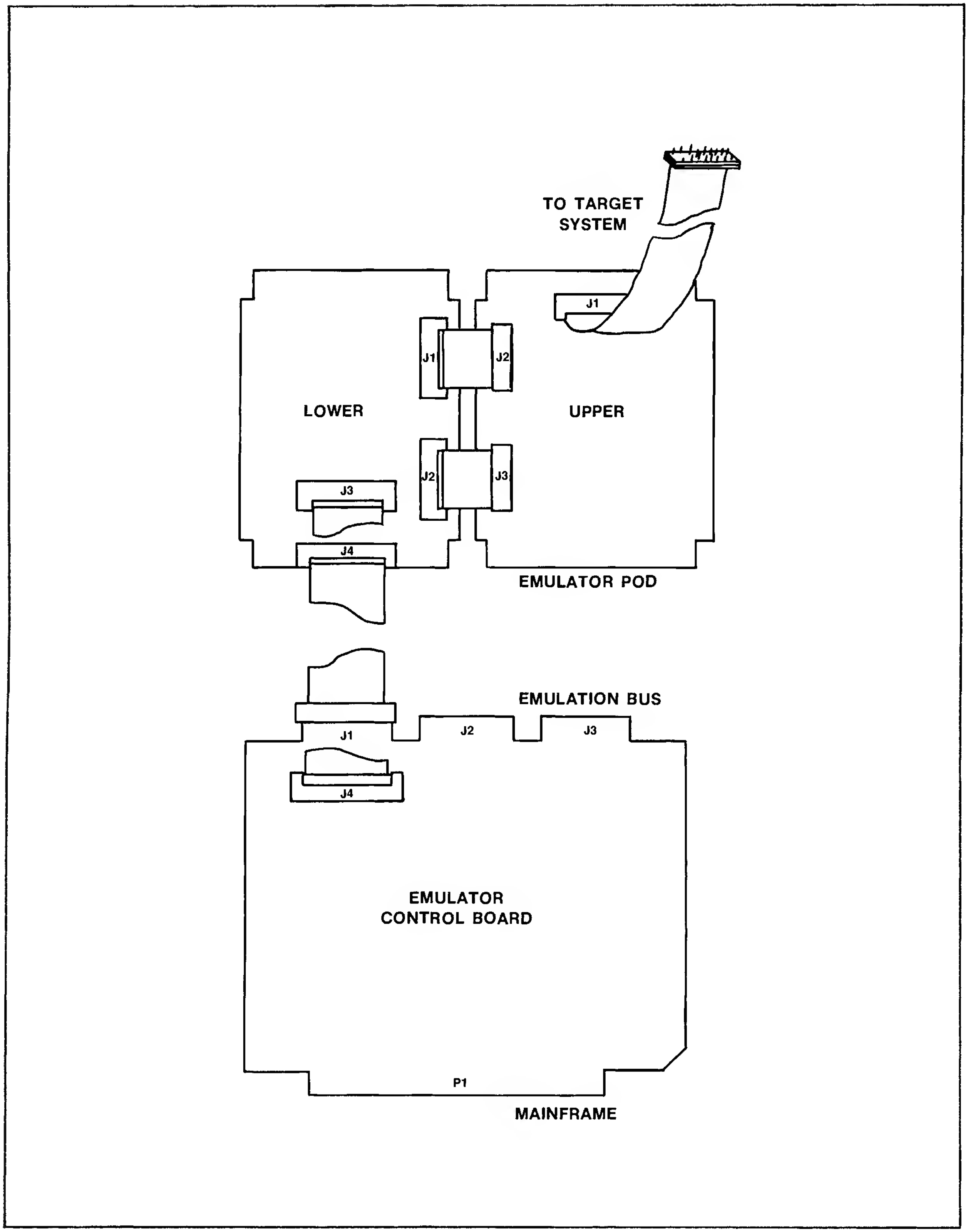


Figure 8-3. Connector Diagram

Table 8-2. Mnemonics

Mnemonic	Description
BLMEM	Buffered Low Memory (pod). Clock from pod processor. When low, address lines contain valid address. When high, data lines contain valid data. See also LMEM and HMEM. Schematics 2, 5, 6, 7*.
HBG	High Background. Indicates the emulator is executing in background memory. It is the complementary signal of HFG. Schematics 5, 6*.
HBGMEM	High Background Memory. Indicates the memory access is to background memory. It is inverted LBGMEM. Schematics 2, 6*.
HBPC	High BPC. Indicates the development station is accessing controller memory. It is inverted LBPC. Schematics 1, 2*, 3, 4.
HBRKREG	High Break Register. On rising edge, clocks the break register; latches break option bits sent by the development station. Schematics 1, 2*.
HDEFIB	High Defibrillate. Inverted LDEFIB; passed to attached pod to initialize it to a known state. Schematic 7.
HFG	High Foreground. Indicates the emulator is executing in foreground memory. It is inverted LFG. Schematics 1, 6*, 7.
HFGMEM	High Foreground Memory. Indicates the memory access is to foreground memory. Schematics 3, 5, 6*, 7.

* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
HGUARD	High Guarded Memory. Indicates an attempt by the emulator processor to access memory beyond limits of the microcomputer being emulated. When low, the access is within valid memory range. Schematics 4*, 5.
HINT	High Internal Memory. Indicates the emulator processor is accessing the foreground memory above address 63, ie., memory internal to the controller. When low, indicates an access to foreground memory below 64, ie, on-chip user memory. Schematics 3, 4*, 5.
HLASTCYCLE	High Last Cycle. Indicates the emulator processor is executing the last machine cycle of an opcode. Complementary signal to LLASTCYCLE. Schematics 2, 6, 7*.
HMEM	High Memory (pod). Clock from pod processor. When high, address lines contain valid address. When high, data lines contain valid data. it is inverted LMEM. See also BLMEM. Schematics 5, 6, 7*.
HMEMBRK	High Memory Break. Control bit from development station; initializes break logic to stop the emulator when an illegal memory operation occurs. Schematics 1*, 5.
HMR	High Memory Request. Indicates the development station wants to access controller memory. It can be tested on TP 5, HMR. Schematic 2.
HOPFETCH	High Opcode Fetch. Indicates the emulator processor is fetching an opcode from memory. Schematics 5, 6, 7*.
HOPTREG	High Pod Option Register. On rising edge, clocks the pod option register; latches pod option bits sent by the development station. Schematics 1, 2*.
	* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
HPORTWRT	High Port Write. Indicates the emulator processor is writing to an address less than 16, ie., port/timer on-chip addresses. Schematics 2*, 6.
HPWRT	High Pod Write. Indicates the emulator processor is writing to memory. Schematic 2.
HRAM	High RAM. Indicates the emulator processor is accessing memory that is mapped as RAM. When low, indicates the access is that is mapped as ROM. Schematics 2, 4*, 5.
HREAD	High Read (pod). Indicates the emulator processor is reading data. It is derived from the LREAD line. Schematics 2, 3, 5, 6, 7*.
HSTATCLK	High Status Register Clock. On rising edge, clocks the emulator status register; latches status bits to be read by the development station. Schematics 1, 6*.
HTIMER	High Timer. Signal directly from user target system plug. Enables timer circuitry on the pod to count. It is used on the controller as a bit to indicate timer status. Schematics 1, 7*.
HUSER	High User. Indicates an emulator processor access to memory below 16. It is inverted LUSER. Can be tested on TP2, USER. Schematic 7.
LA0-15	Low Address Bus 0-15. Address bus from the development station processor. Uses negative logic; high = 0, low = 1. Schematic 1.
	* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonics	Description
LA0	Low Address Line 0. Address line from development station. It is decoded to determine the controller memory register being accessed. Uses negative logic; high = 0, low = 1. Schematics 1*, 2.
LA1	Low Address Line 1. Address line from development station. It is decoded to determine the controller register being accessed. Uses negative logic; high = 0, low = 1. Schematics 1*, 2.
LA12	Low Address Line 12. Address line from development station. It is decoded to determine if foreground or background memory is being accessed. Uses negative logic; high = 0, low = 1. Schematics 1*, 2.
LA13	Low Address Line 13. Address line from development station. It is decoded to determine if the controller registers are being accessed. Schematics 1*, 2, 3.
LADDREG	Low Address Register. Enables last-address register to drive LD0-15 data bus. Schematics 2*, 5.
LANAL	Low Analysis. Indicates to an attached internal analyzer option card that the emulation bus contains valid emulation information. Schematic 7.
LBADOPC	Low Bad Opcode. Indicates an invalid opcode has been detected. Schematics 5, 7*.
LBGMEM	Low Background Memory. Indicates the memory access is to background memory. See also HBGMEM. Schematics 3, 6*.
	* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonics	Description
LBPC	Low BPC. Indicates the development station is accessing controller memory. When inverted, produces HBPC. It can be tested on TP1, BPC. Schematics 1, 2*, 3, 5.
LBPCBRK	Low BPC break. Signal from development station that forces the emulator processor into background memory. Schematics 1*, 5.
LBREAK	Low Break. Indicates an emulation break has occurred. Schematics 5*, 6.
LD0-15	Low Data Bus 0-15. Bidirectional data bus between the controller and the development station. Uses negative logic; high = 0, low = 1. Schematics 1*, 5*.
LDATAIN	Low Data In. Enables the development station to drive the LED0-7 data bus, ie., data comes into the controller. Schematics 1, 2*.
LDATAOUT	Low Data Out. Enables the emulator controller to drive the LED0-7 data bus, ie., data goes out of the controller. Schematics 1, 2*.
LDEFIB	Low Defibrillate. Signal from the development station that initializes the controller to a known state. When inverted, becomes HDEFIB. Schematics 1*, 2, 6, 7.
LEA0-12	Low Emulator Address Bus 0-12. Thirteen low order bits of LEA0-15. Determines address within 1K blocks of foreground and background memory. Uses negative logic; high = 0, low = 1. Schematics 3, 4*, 6.

* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonics	Descriptions
LEA0-15	Low Emulator Address Bus 0-15. Address lines used by the emulator processor. Can be monitored by attached internal analyzer option card. These lines can also be driven by the development station to access controller memory. Uses negative logic; high = 0, low = 1. Schematics 1*, 4*, 5.
LEBRK	Low Emulator Break. Indicates an internal analysis option card is requesting the emulator to stop running in foreground memory. Schematics 5, 7*.
LED0-3	Low Emulator Data Bus 0-3. Four low order bits of LED0-7. Used to load the user memory operation counter. Schematics 1*, 3, 4, 6, 7.
LED0-7	Low Emulator Data Bus 0-7. Data bus used by the emulator processor. Can be monitored by attached internal analyzer option card. These lines can also be driven by the development station. Uses negative logic; high = 0, low = 1. Schematics 1*, 3, 4*, 7.
LEMID	Low Emulator Identification. Enables controller to drive the LD0-7 data bus with the controller and attached pod identification codes. Schematics 1, 2*.
LES0-3	Low Emulator Status Bus 0-3. Status bits made available to an attached internal analyzer option card; bit 0 = OPFETCH, 1 = LREAD, 2 = opcode status, 3 = opcode status. Schematic 7.
LES2	Low Emulator Status Line 2. Indicates opcode status. Schematics 5, 7*.

* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
LEXT	Low External. Signal from development station; when low, selects external clock source on the users target system. When high, selects 4 MHz crystal located on the pod. Schematics 1*, 7.
LFG	Low Foreground. Indicates the emulator is executing in foreground memory. When inverted produces HFG. It is available on TP6, FG. Schematic 7.
LICE	Low In-ciruit Emulation. Status bit from attached pod. Indicates target system plug is receiving +5v from user hardware. Schematics 1, 7*.
LID	Low Identification Request. Signal from development station; requests emulator identification be placed on the LDO-7 data bus. Also, see LEMID. Schematics 1*, 2.
LILLMEM	Low Illegal Memory. Indicates an error in addressing controller memory, such as a write to ROM-mapped memory or address out of range. Schematics 1, 5*.
LILLOPC	Low Illegal Opcode. Indicates the emulator processor has attempted to execute an illegal opcode. Schematics 1, 5*, 6.
LIRQ	Low Interrupt Request. Signal directly from target system plug; indicates the user hardware has issued an interrupt request. It is used by the controller as a bit to show processor status. Schematics 1, 7*
LJAM	Low Jam. Enables the controller to jam the software interrupt opcode SWI onto the data bus to the attached pod. It can be tested on TP4, JAM. Schematics 4, 5, 6*.
	* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonics	Description
LLASTCYCLE	Low Last Cycle. Indicates the emulator processor is executing the last machine cycle of an opcode. Complementary signal to HLASTCYCLE. Schematics 6, 7*.
LMEM	Low Memory (pod). Clock from pod processor. When low, address lines contain valid address. When high, data lines contain valid data. See also BLMEM and HMEM. It can be tested on TP3, LMEM. Schematics 5, 7*.
LMEMMON	Low Memory Monitor. Enables memory access monitor RAM to be loaded with data. Schematics 2*, 4.
LMSYN	Low Memory Synchronization. Signal to development station; forces station to delay access to controller memory, until emulator processor has completed its memory access. Schematics 1, 2*.
LNCLK	Low No-clock. Indicates slow, or no clock, in the emulator pod. Schematics 1, 2*.
LOPCBRK	Low Opcode Break. Signal from development station that initializes controller break logic. Causes emulation break whenever an illegal opcode is found. Schematics 1*, 5.
LOPCREG	Low Opcode Register. Enables last-opcode register to drive the LD0-15 data bus; places the address of the last executed opcode on the bus. Schematics 2*, 5.
LPODIN	Low Pod Data In. Gates data from the attached pod onto the controller LED0-7 data bus. Schematics 4, 5*.
	* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonics	Description
LPODOUT	Low Pod Data Out. Gates data from the controller out to the attached pod. Schematics 4, 5*.
LPOPT0-7	Low Pod Option Bus 0-7. Option control bits from the development station. The controller passes the bits to the attached pod. Schematics 1*, 7.
LPORTS	Low Ports. Indicates the emulator processor is accessing memory in the range 0-15. These addresses are primarily for ports/timer. Schematics 2, 4*, 7.
LPSTAT0-7	Low Pod Status Bus 0-7. Indicate status of attached pod. The following bits have specific assigned names: 0 = LRESET, 1 = LIRQ, 2 = HTIMER, 7 = LICE. Some bits function depend upon the attached emulator. Uses negative logic; high = 0, low = 1. Schematics 1, 7*.
LPSTAT3-6	Low Pod Status Bus 3-6. Variable function bits showing pod status. See LPSTAT0-7. Uses negative logic; high = 0, low = 1. Schematics 1, 7*.
LREAD	Low Read. Indicates the emulator processor is reading data. When inverted, becomes HREAD. Schematic 7.
LRESET	Low Reset. Status bit from attached pod; indicates the emulator processor is reset. Schematics 1, 7*.
LRESET1	Low Reset 1. Derived from LRESET; resets user memory operation cycle counter, and illegal memory flip-flop. Schematics 5, 7*.
	* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonics	Description
LROMBRK	Low ROM Break. Signal from development station that initializes break logic. Whenever the emulator processor attempts to write to memory mapped as ROM, the emulator stops. Schematics 1*, 5.
LSEL	Low Select. Signal from development station; indicates the controller is selected. Schematics 1*, 2.
LSTATREG	Low Status Register. Enables emulator status buffer to drive the LD0-7 data bus, ie., the controller writes the status to the development station. Schematics 1, 2*, 6.
LSTB	Low Strobe. Signal from development station; when low and in the write mode, indicates station is driving LD0-15 data bus. When low and in the read mode, it indicates that the controller can drive the data bus. Schematics 1*, 2.
LSTM	Low Start Memory. Signal from the development station; indicates the station is driving the LD0-15 data bus. Schematics 1*, 2.
LUSER	Low User. Indicates an emulator processor access to memory below 63. When inverted it produces HUSER. Schematics 5*, 7.
LWE	Low Write Enable. Enables foreground and background memory to be written to. Can be tested on TP 7, WE. Schematics 2*, 3.
LWRT	Low Write. Signal from development station; indicates the station is attempting to write to controller memory.
	* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonics	Description
PIDO-3	Pod Identification Bus 0-3. Four bits that uniquely identify the attached emulator pod. Originates on the pod and is passed by the controller to the development station on the LDO-15 data bus. Schematics 1, 7*.

* indicates signal source.

Table 8-3. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

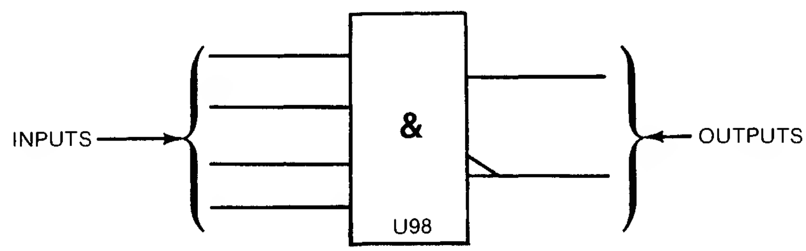
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

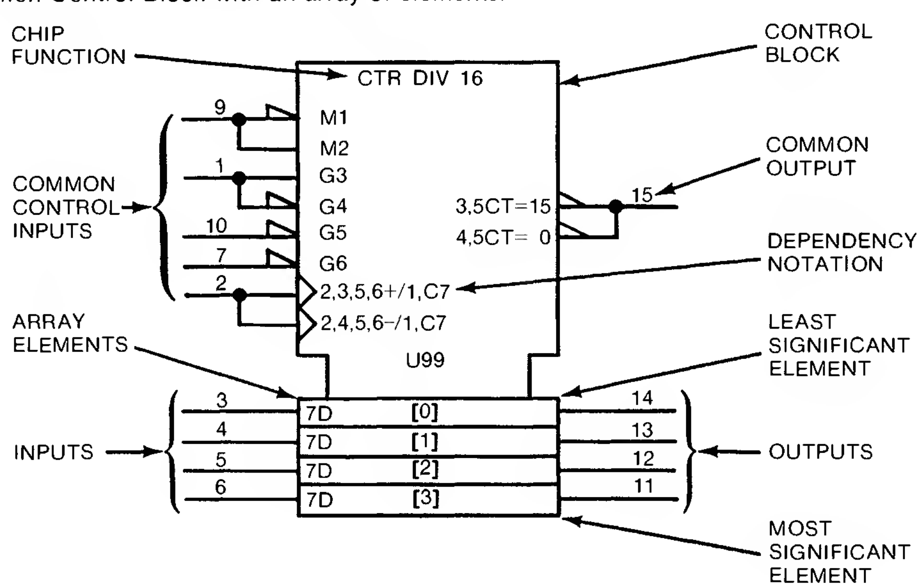
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in [ ]).

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Table 8-3. Logic Symbols (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (complements state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-3. Logic Symbols (Cont'd)

OTHER SYMBOLS

∩	Analog Signal
&	AND
} {	Bit Grouping
▷	Buffer
!	Compare
▷	Dynamic
=1	Exclusive OR
	Hysteresis
?	Interrogation
—	Internal Connection
	Inversion
O	Negation
	Nonlogic Input/Output
	Open Circuit (external resistor)
	Open Circuit (external resistor)
≥1	OR
	Passive Pull Down (internal resistor)
	Passive Pull Up (internal resistor)
˥	Postponed
←	Shift Left (or up)
→	Shift Right (or down)
/	Solidus (allows an input or output to have more than one function)
▽	Tri-State
,	Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
( )	Used for factoring terms using algebraic techniques.
[ ]	Information not defined.
Φ	Logic symbol not defined due to complexity.

LABELS

BG	Borrow Generate
BI	Borrow Input
BO	Borrow Output
BP	Borrow Propagate
CG	Carry Generate
CI	Carry Input
CO	Carry Output
CP	Carry Propagate
CT	Content
D	Data Input
E	Extension (input or output)
F	Function
J	J Input
K	K Input
P	Operand
T	Transition
+	Count Up
-	Count Down

MATH FUNCTIONS

Σ	Adder
ALU	Arithmetic Logic Unit
COMP	Comparator
DIV	Divide By
=	Equal To
>	Greater Than
<	Less Than
CPG	Look Ahead Carry Generator
π	Multiplier
P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal
BIN	Binary
BUF	Buffer
CTR	Counter
DEC	Decimal
DIR	Directional
DMUX	Demultiplexer
FF	Flip-Flop
MUX	Multiplexer
OCT	Octal
RAM	Random Access Memory
RCVR	Line Receiver
ROM	Read Only Memory
SEG	Segment
SRG	Shift Register

DELAY and MULTIVIBRATORS

	Astable
100 ns	Delay
1	Nonretriggerable Monostable
NV	Nonvolatile
	Retriggerable Monostable

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Table 8-4. Schematic Diagram Notes

	ETCHED CIRCUIT BOARD
	FRONT PANEL MARKING
	REAR-PANEL MARKING
	MANUAL CONTROL
	SCREWDRIVER ADJUSTMENT
TP1	ELECTRICAL TEST POINT TP (WITH NUMBER)
1	NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.
A	LETTERED TEST POINT NO MEASUREMENT AID PROVIDED
A	COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.
1 3	NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION. LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.
A	CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.
	INDICATES SINGLE SIGNAL LINE

(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

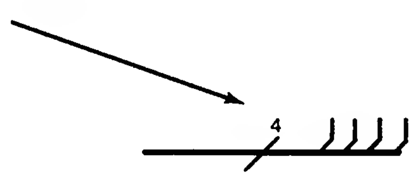
0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

µP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

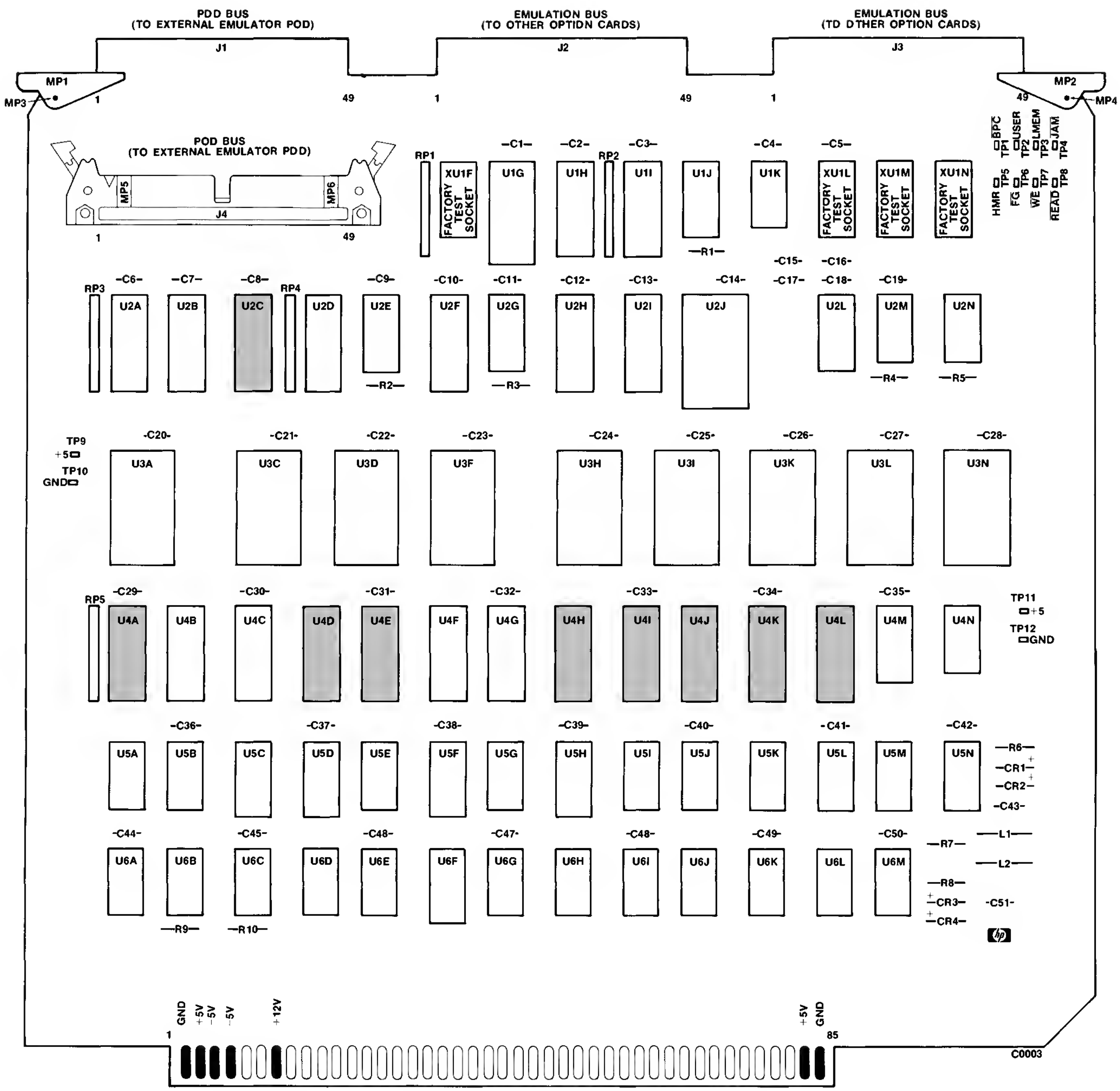
NUMBER OF LINES ON A BUS

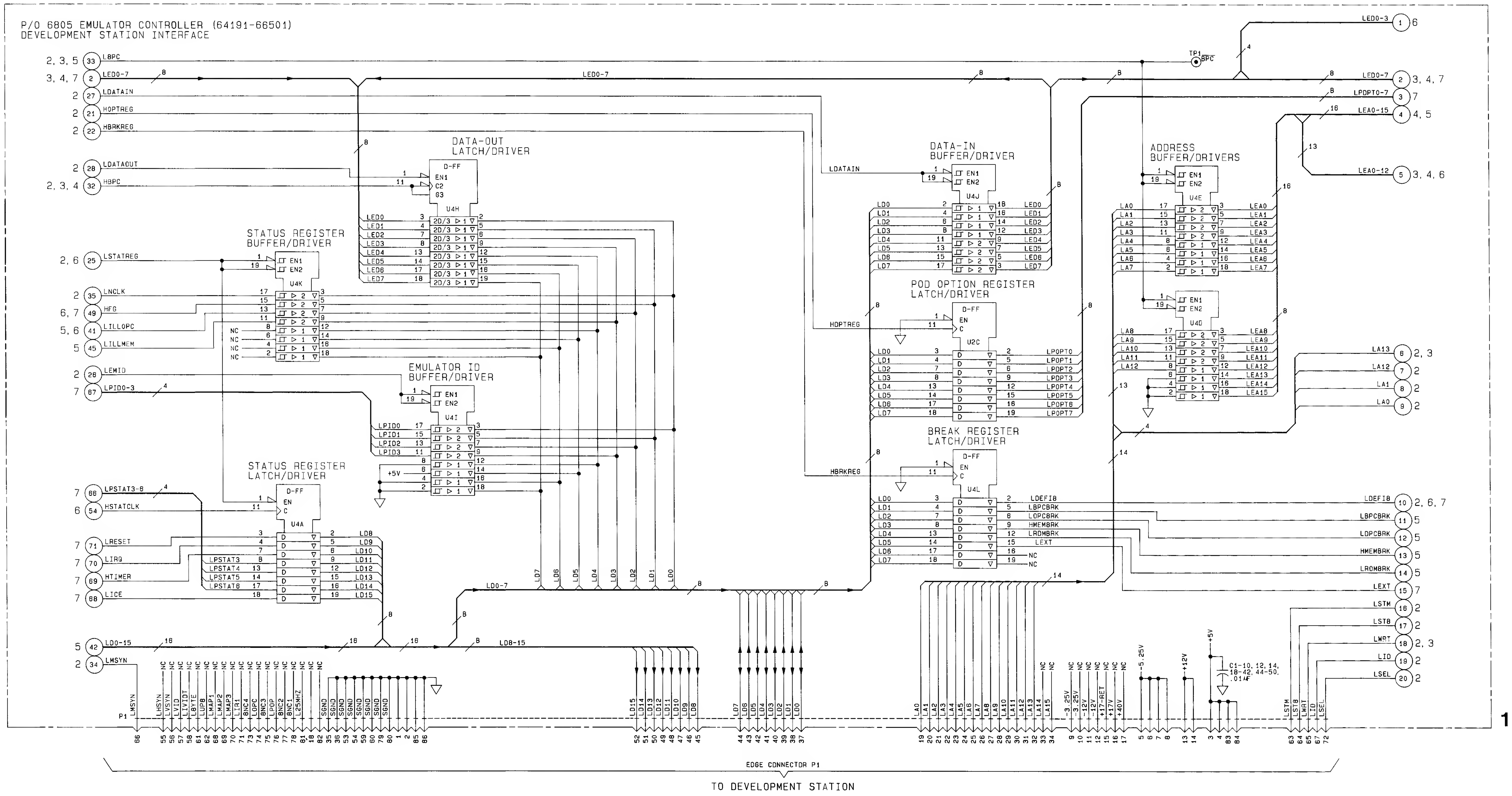


STD-20-09-81

Table 8-5. IC To Schematic Cross-Reference

IC	Schematic	IC	Schematic
U1G	4	U5A	7
U1H	4	U5B	5
U1I	4	U5C	3
U1J	7	U5D	7
U1K	5	U5E	7
		U5F	2
U2A	7	U5G	6
U2B	4, 7	U5H	6
U2C	1	U5I	3
U2D	4	U5J	2
U2E	4	U5K	2
U2F	4	U5L	2
U2G	2	U5M	2, 5, 6
U2H	4	U5N	2
U2I	7		
U2J	7	U6A	2, 5
U2L	7	U6B	2, 5
U2M	5, 7	U6C	5
U2N	5	U6D	6, 7
		U6E	6, 7
U3A	3	U6F	6
U3C	3	U6G	6
U3D	3	U6H	2, 6
U3F	3	U6I	2, 6
U3H	3	U6J	2, 7
U3I	3	U6K	2
U3K	3	U6L	2
U3L	3	U6M	2
U3N	3		
U4A	1		
U4B	5		
U4C	5		
U4D	1		
U4E	1		
U4F	5		
U4G	5		
U4H	1		
U4I	1		
U4J	1		
U4K	1		
U4L	1		
U4M	6		
U4N	2, 3		





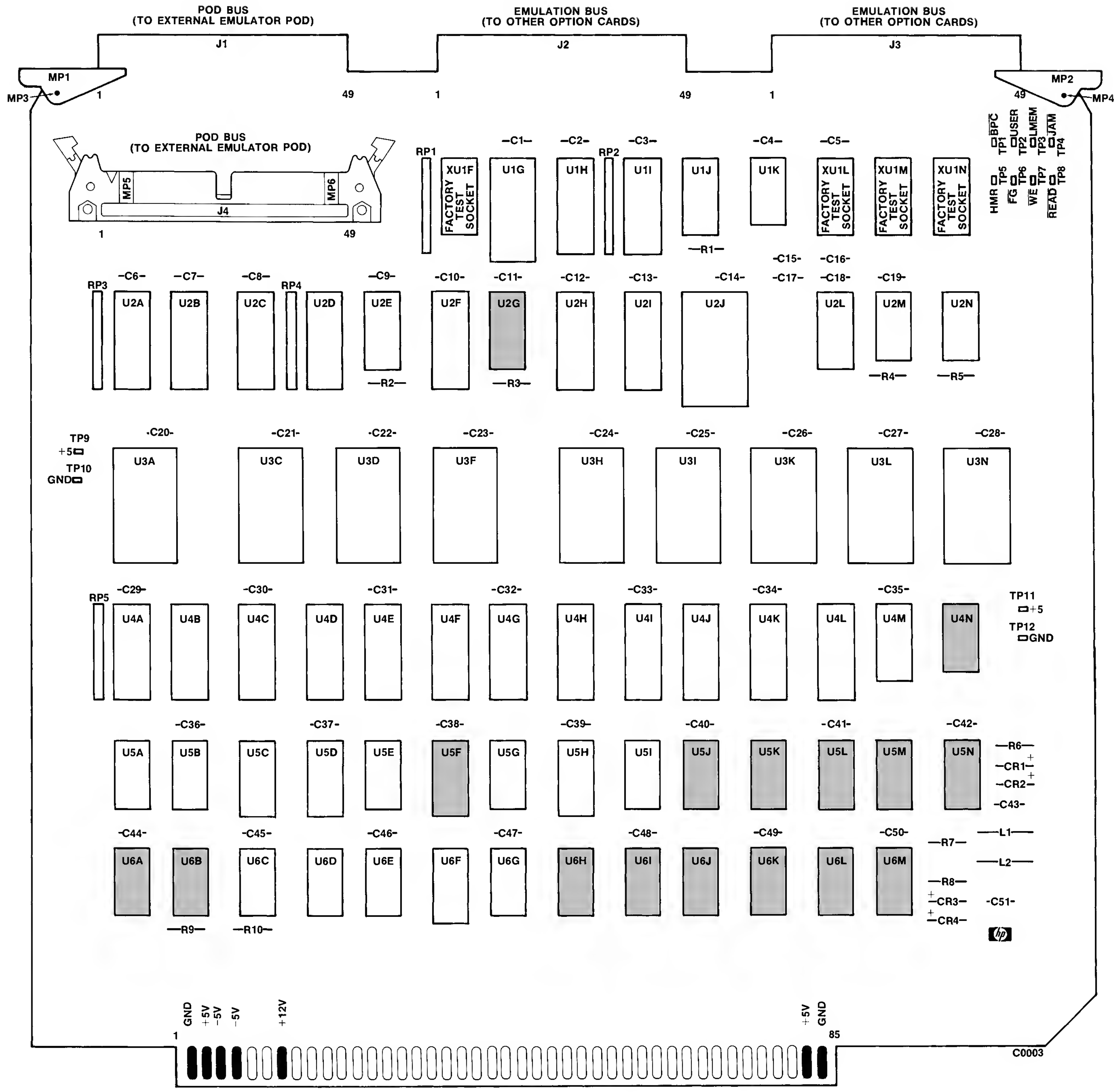
ICs On This Schematic

REF DES	HP PART NUMBER	MFG. PART NUMBER	+5V PIN	GND PIN
U2C	1820-1997	SN74LS374N	20	10
U4A	1820-1997	SN74LS374N	20	10
U4D	1820-2024	SN74LS244N	20	10
U4E	1820-2024	SN74LS244N	20	10
U4H	1820-2102	SN74LS373N	20	10
U4I	1820-1917	SN74LS240N	20	10
U4J	1820-2024	SN74LS244N	20	10
U4K	1820-2024	SN74LS244N	20	10
U4L	1820-1997	SN74LS374N	20	10

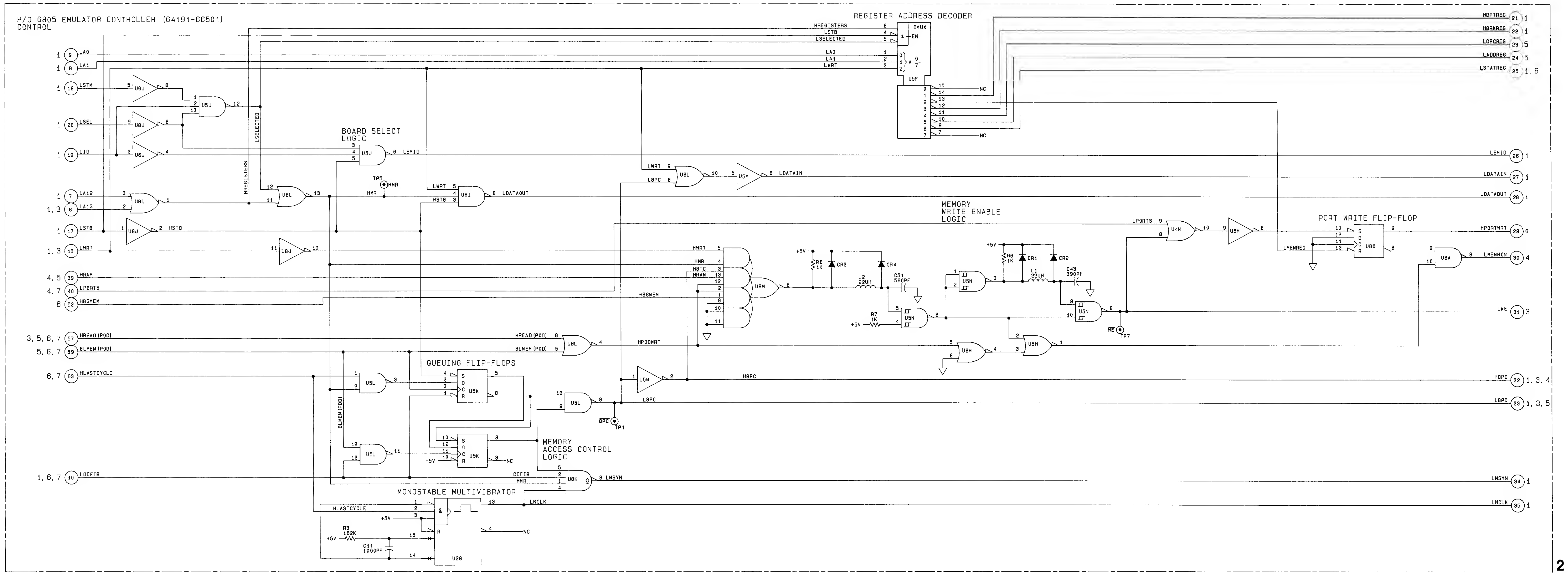
Parts On This Schematic

C1-10,12,14,15,18-42,44-50.

Figure 8-4. Schematic 1
Development Station Interface



Component Locator



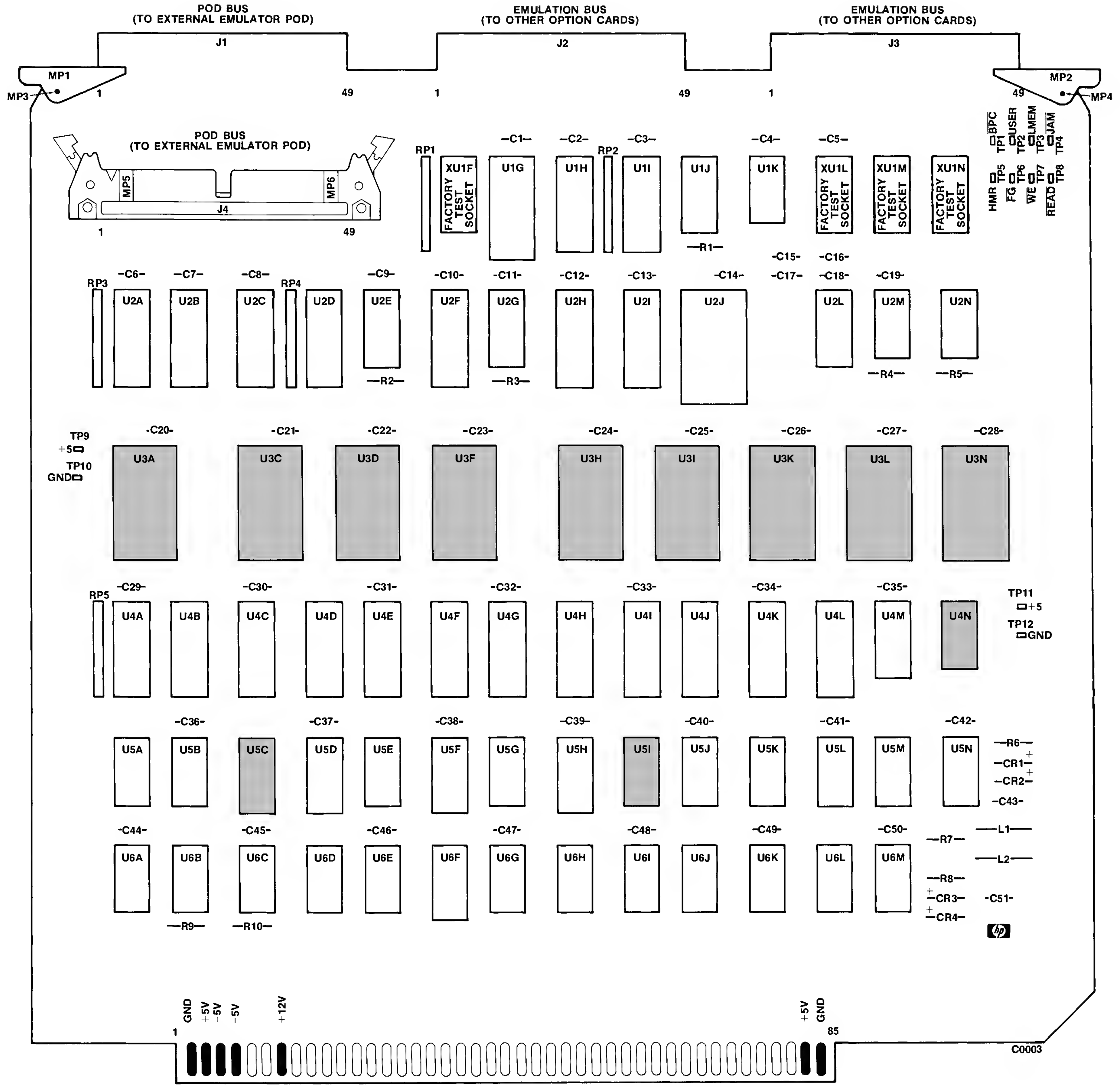
ICs On This Schematic

REF. DES	HP PART NUMBER	MFG. PART NUMBER	+5V PIN	GND PIN
U2G	1820-1423	SN74LS123N	16	8
U4N	1820-1144	SN74LS02N	14	7
U5F	1820-1216	SN74LS138N	16	8
U5J	1820-1202	SN74LS10N	14	7
U5K	1820-1112	SN74LS74AN	14	7
U5L	1820-1197	SN74LS00N	14	7
U5M	1820-1199	SN74LS04N	14	7
U5N	1820-1307	SN74S132N	14	7
U6A	1820-1197	SN74LS00N	14	7
U6B	1820-1112	SN74LS74AN	14	7
U6H	1820-1144	SN74LS02N	14	7
U6I	1820-1202	SN74LS10N	14	7
U6J	1820-1199	SN74LS04N	14	7
U6K	1820-1274	SN74LS22N	14	7
U6L	1820-1144	SN74LS02N	14	7
U6M	1820-1285	SN74LS54N	14	7

Parts On This Schematic

C1,51,43.	L1,2.
CR1,2,3,4.	R3,6,7,8.

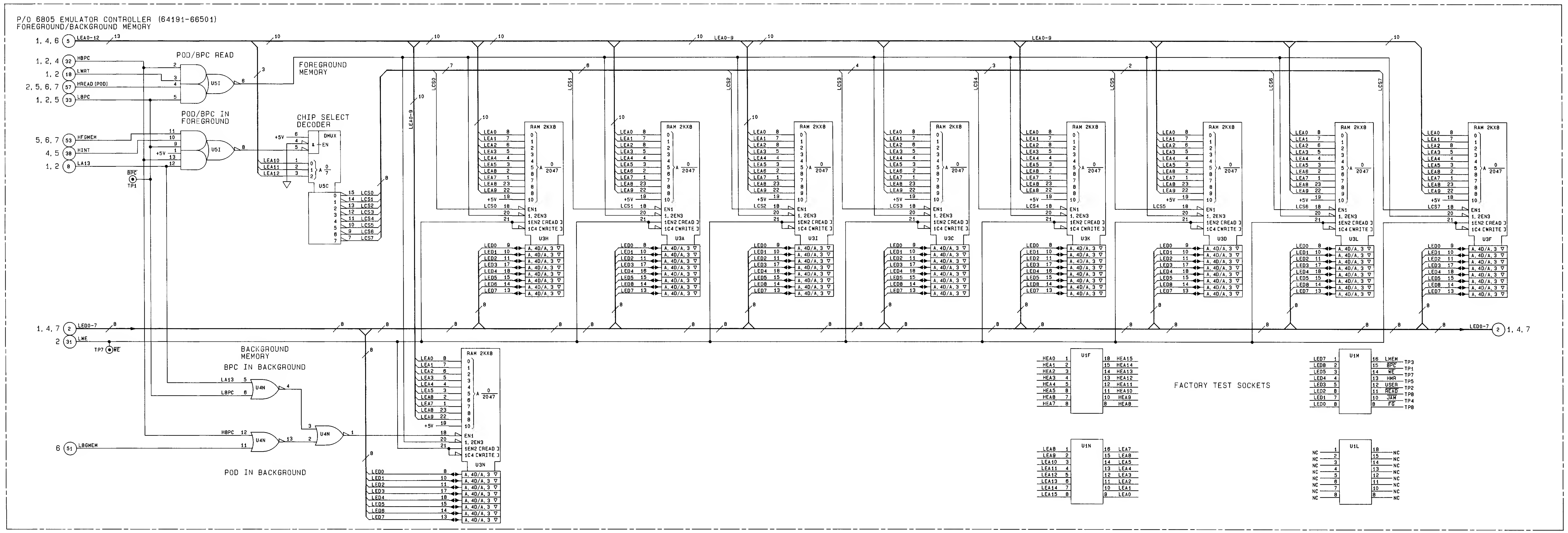
Figure 8-5. Schematic 2
Control



Component Locator

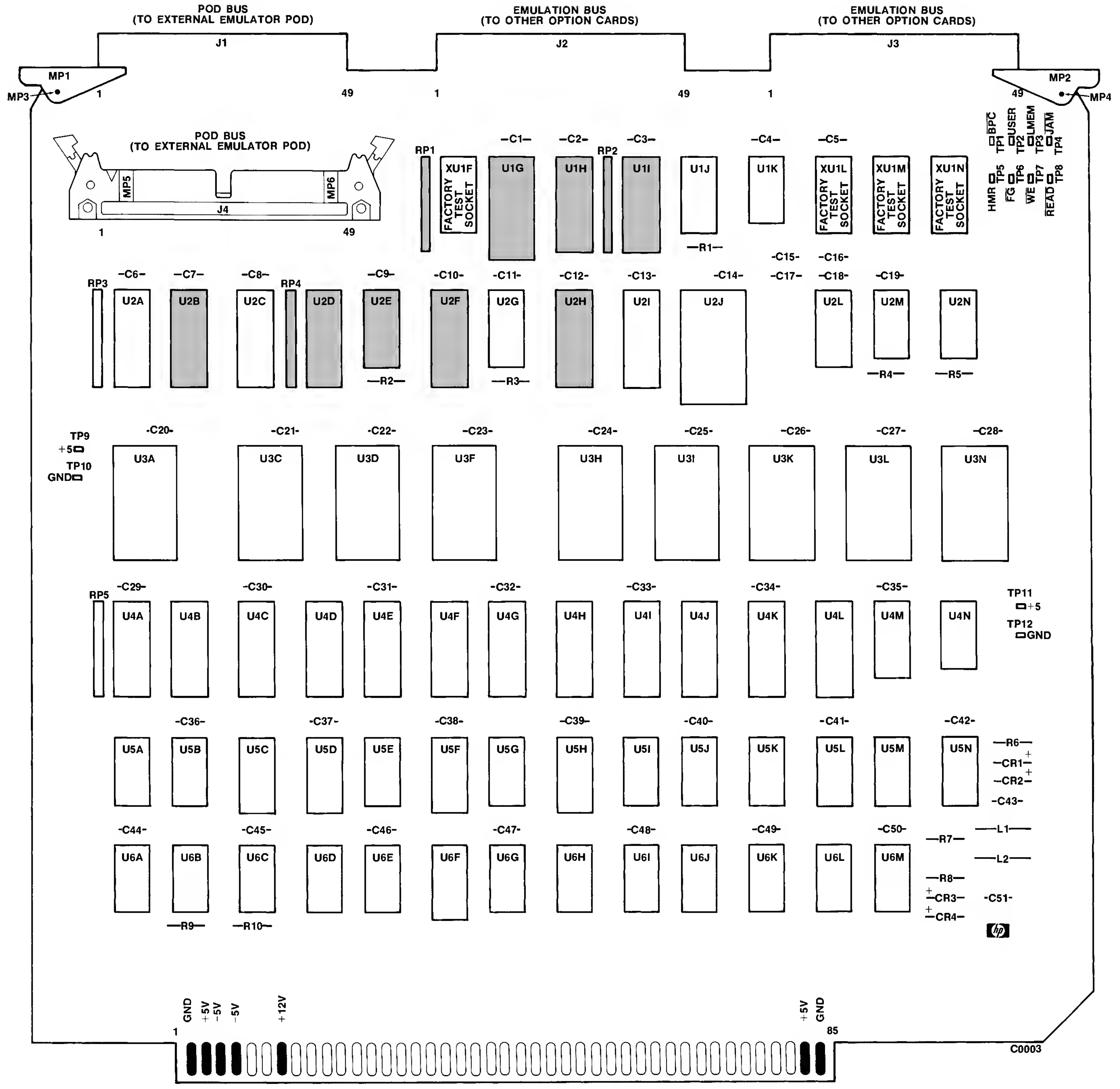
ICs On This Schematic

REF. DES	HP PART NUMBER	MFG. PART NUMBER	+5V PIN	GND PIN
U3A	1818-1611	HM6116P-3	24	12
U3C	1818-1611	HM6116P-3	24	12
U3D	1818-1611	HM6116P-3	24	12
U3F	1818-1611	HM6116P-3	24	12
U3H	1818-1611	HM6116P-3	24	12
U3I	1818-1611	HM6116P-3	24	12
U3K	1818-1611	HM6116P-3	24	12
U3L	1818-1611	HM6116P-3	24	12
U3N	1818-1611	HM6116P-3	24	12
U4N	1820-1144	SN74LS02N	14	7
U5C	1820-1216	SN74LS138N	16	8
U5I	1820-1210	SN74LS51N	14	7

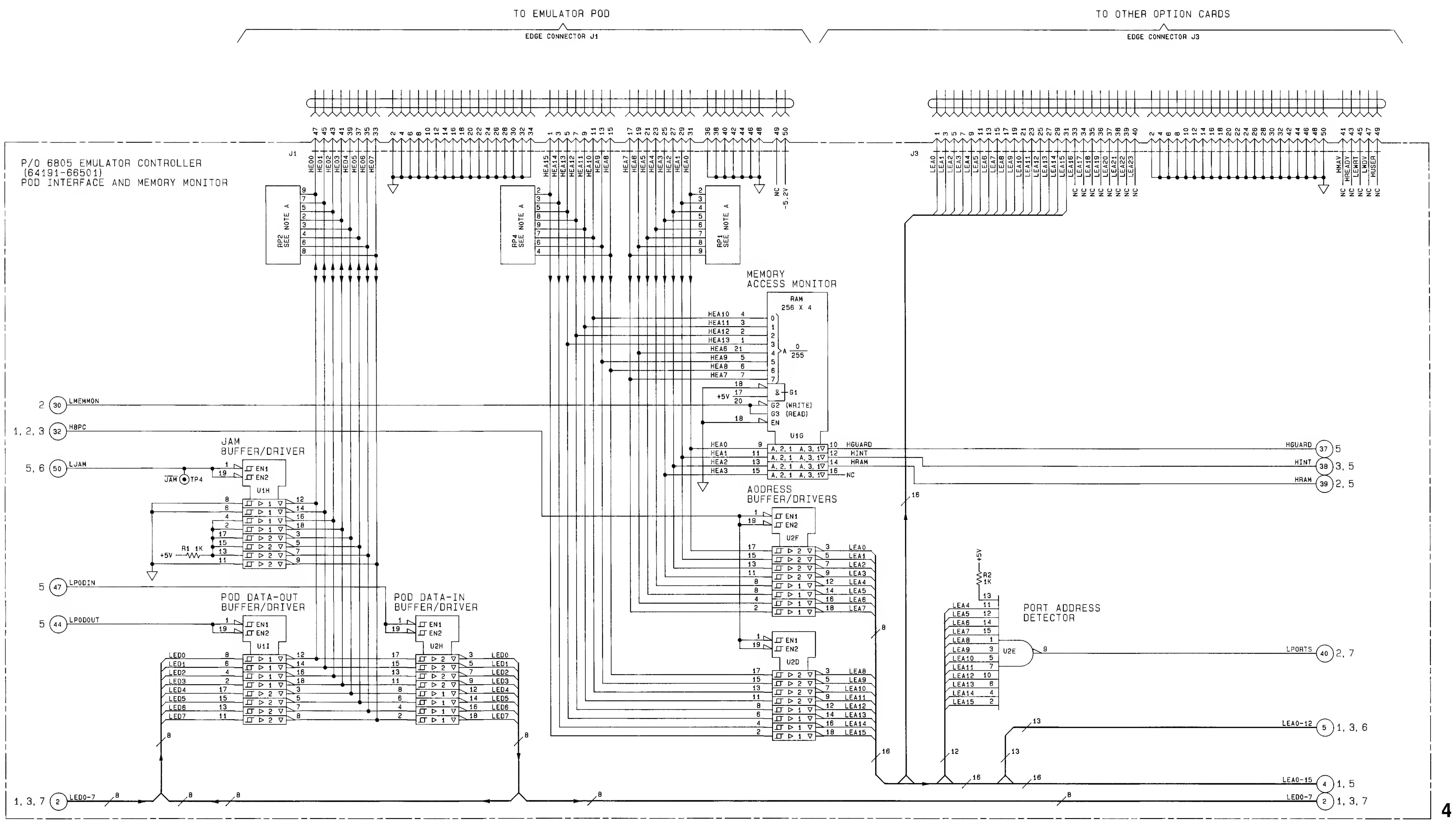


3

Figure 8-6. Schematic 3
Foreground/Background Memory



Component Locator



ICs On This Schematic

REF. DES	HP PART NUMBER	MFG. PART NUMBER	+5V PIN	GND PIN
U1G	1816-1308	93L422PC	22	8
U1H	1820-1633	SN74S240N	20	10
U1I	1820-1633	SN74S240N	20	10
U2B	1820-1633	SN74S240N	20	10
U2D	1820-1917	SN74LS240N	20	10
U2E	1820-1130	SN74S133N	16	8
U2F	1820-1917	SN74LS240N	20	10
U2H	1820-1917	SN74LS240N	20	10

Parts On This Schematic

R1,2.	RP1,2,4.

NOTE A

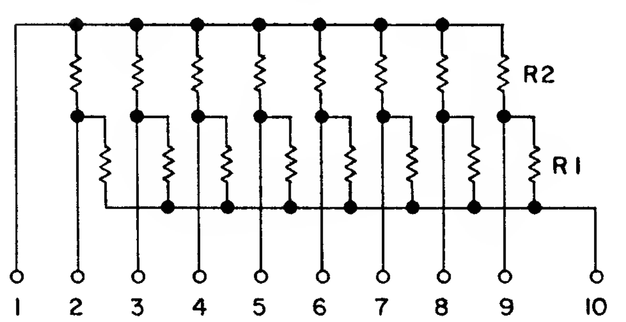
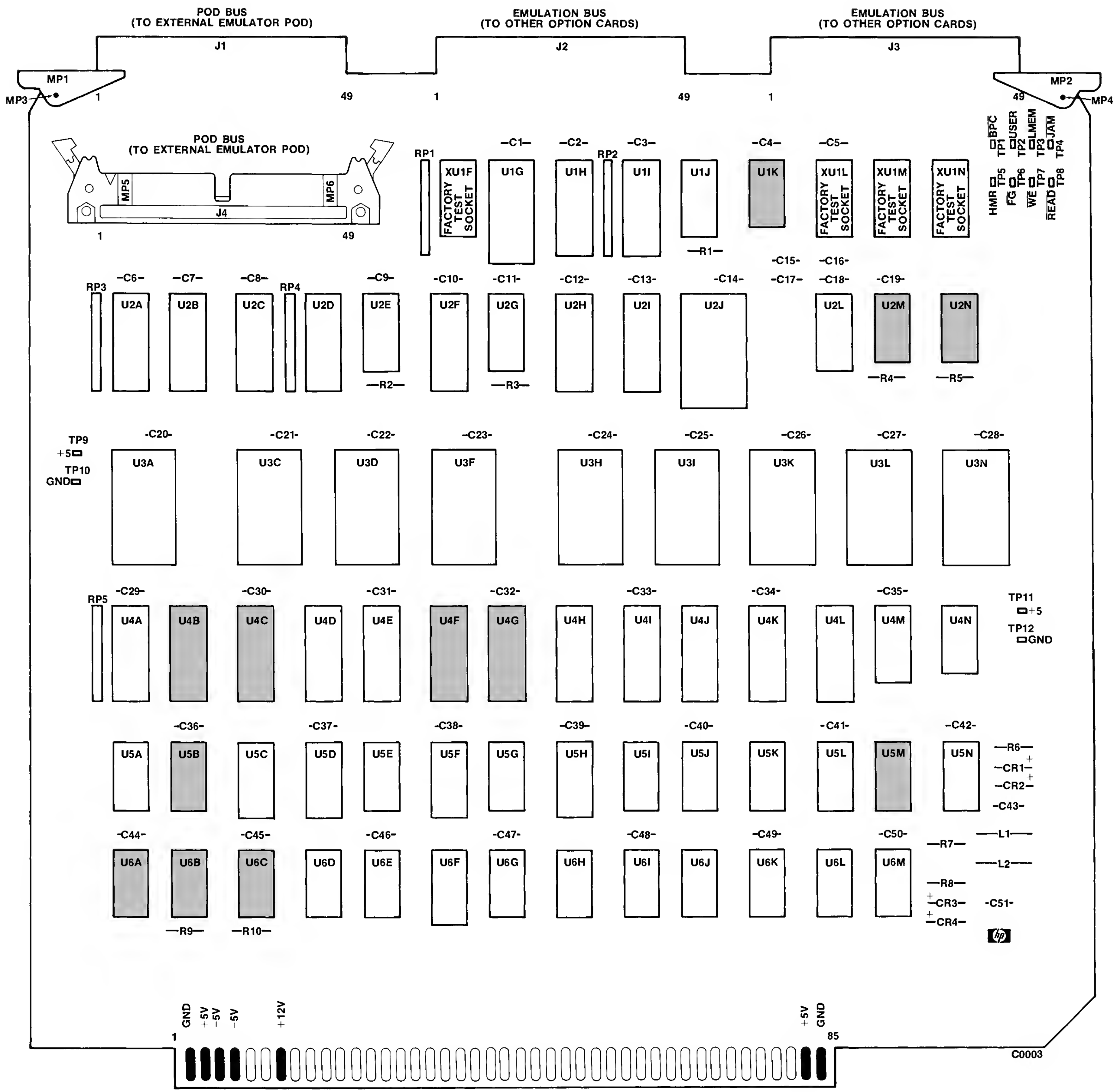
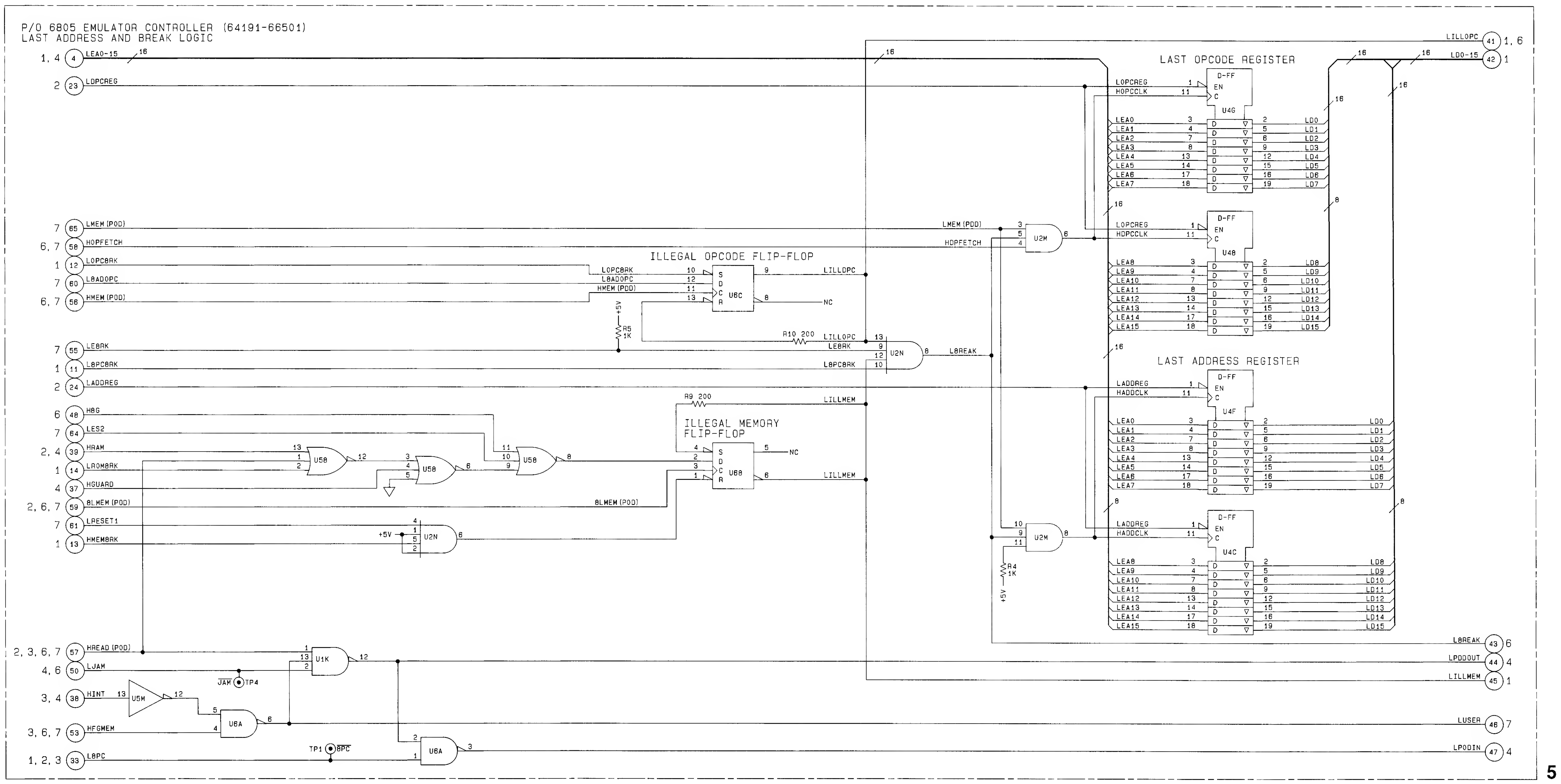


Figure 8-7. Service Sheet 4
Pod Interface and Memory Monitor



Component Locator



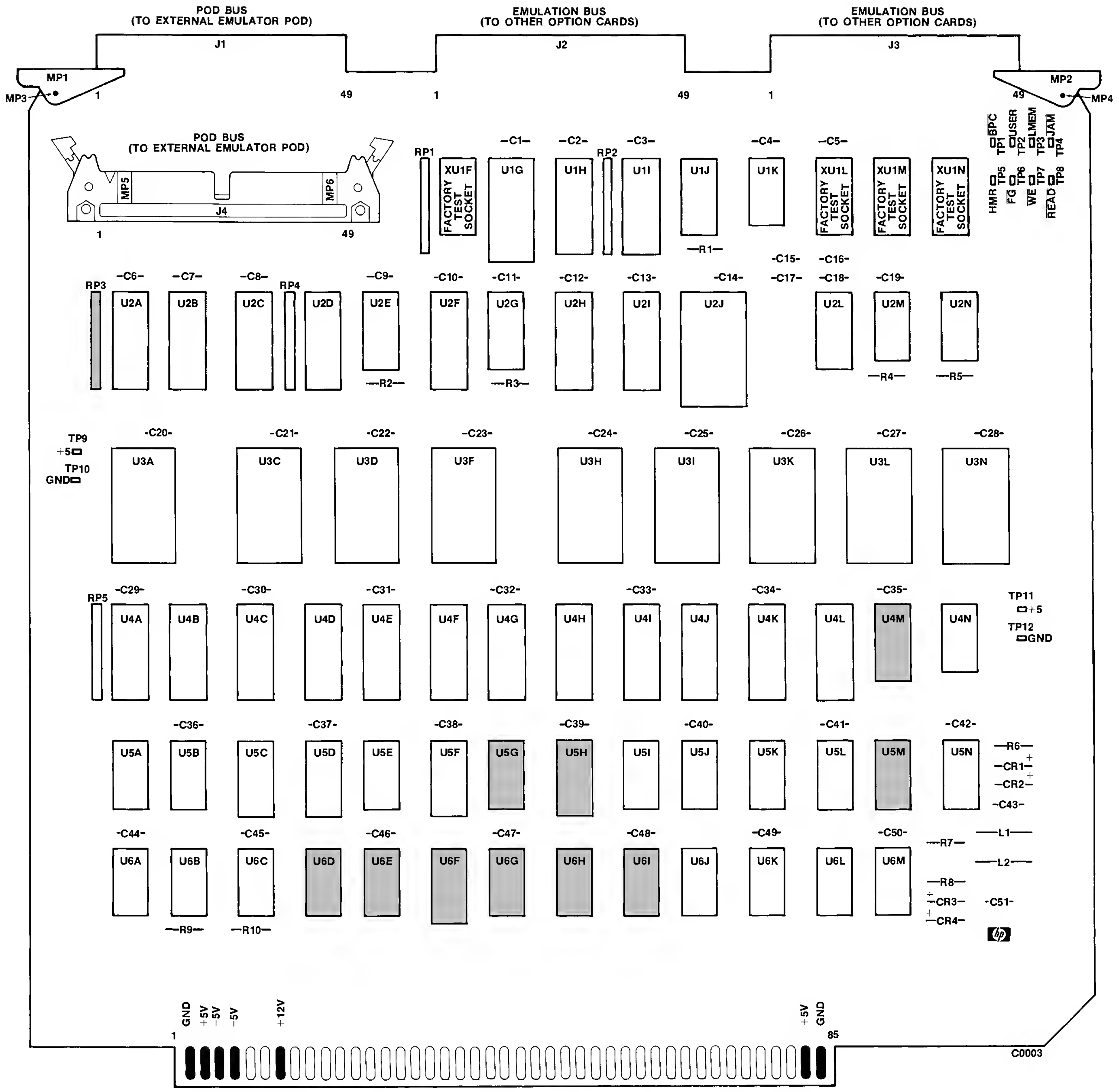
ICs On This Schematic

REF. DES	HP PART NUMBER	MFG. PART NUMBER	+5V PIN	GND PIN
U1K	1820-1202	SN74LS10N	14	7
U2M	1820-0686	SN74S11N	14	7
U2N	1820-1205	SN74LS21N	14	7
U4B	1820-1997	SN74LS374N	20	10
U4C	1820-1997	SN74LS374N	20	10
U4F	1820-1997	SN74LS374N	20	10
U4G	1820-1997	SN74LS374N	20	10
U5B	1820-1206	SN74LS27N	14	7
U5M	1820-1199	SN74LS04N	14	7
U6A	1820-1197	SN74LS00N	14	7
U6B	1820-1112	SN74LS74AN	14	7
U6C	1820-1112	SN74LS74AN	14	7

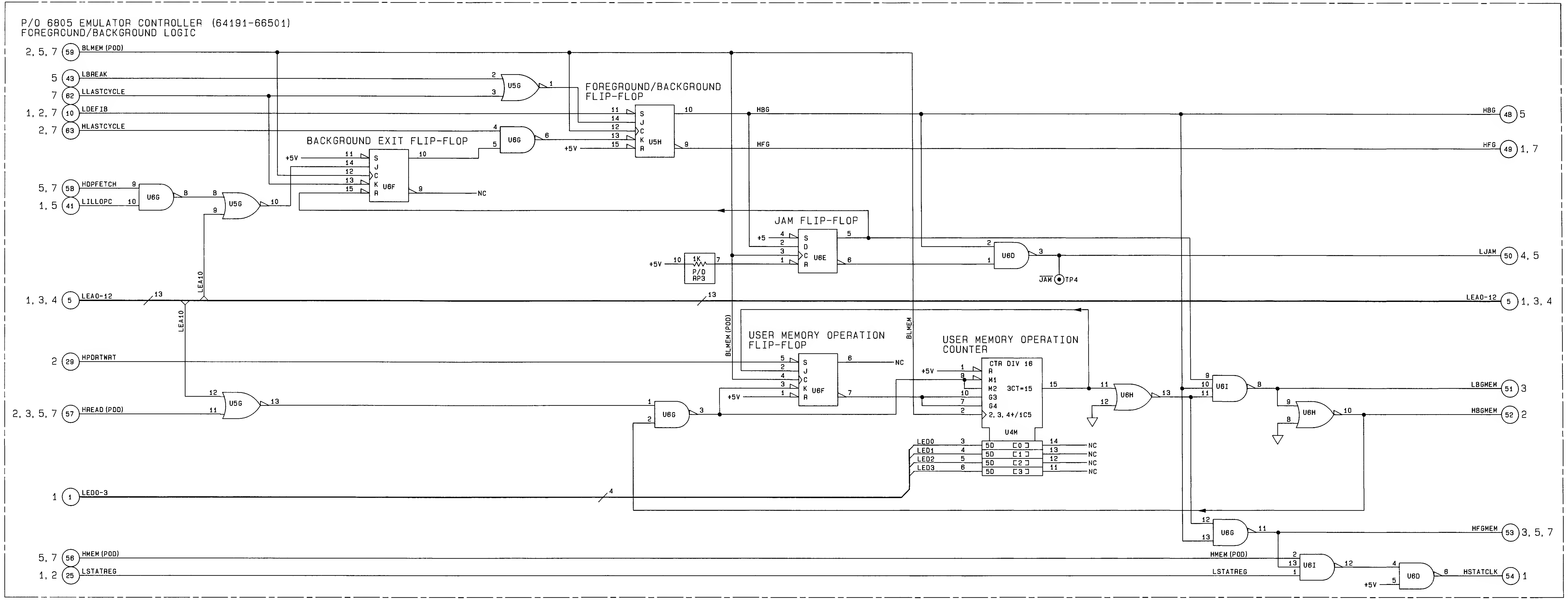
Parts On This Schematic

R4,9,10.

Figure 8-8. Schematic 5
Last Address and Break Logic



Component Locator



6

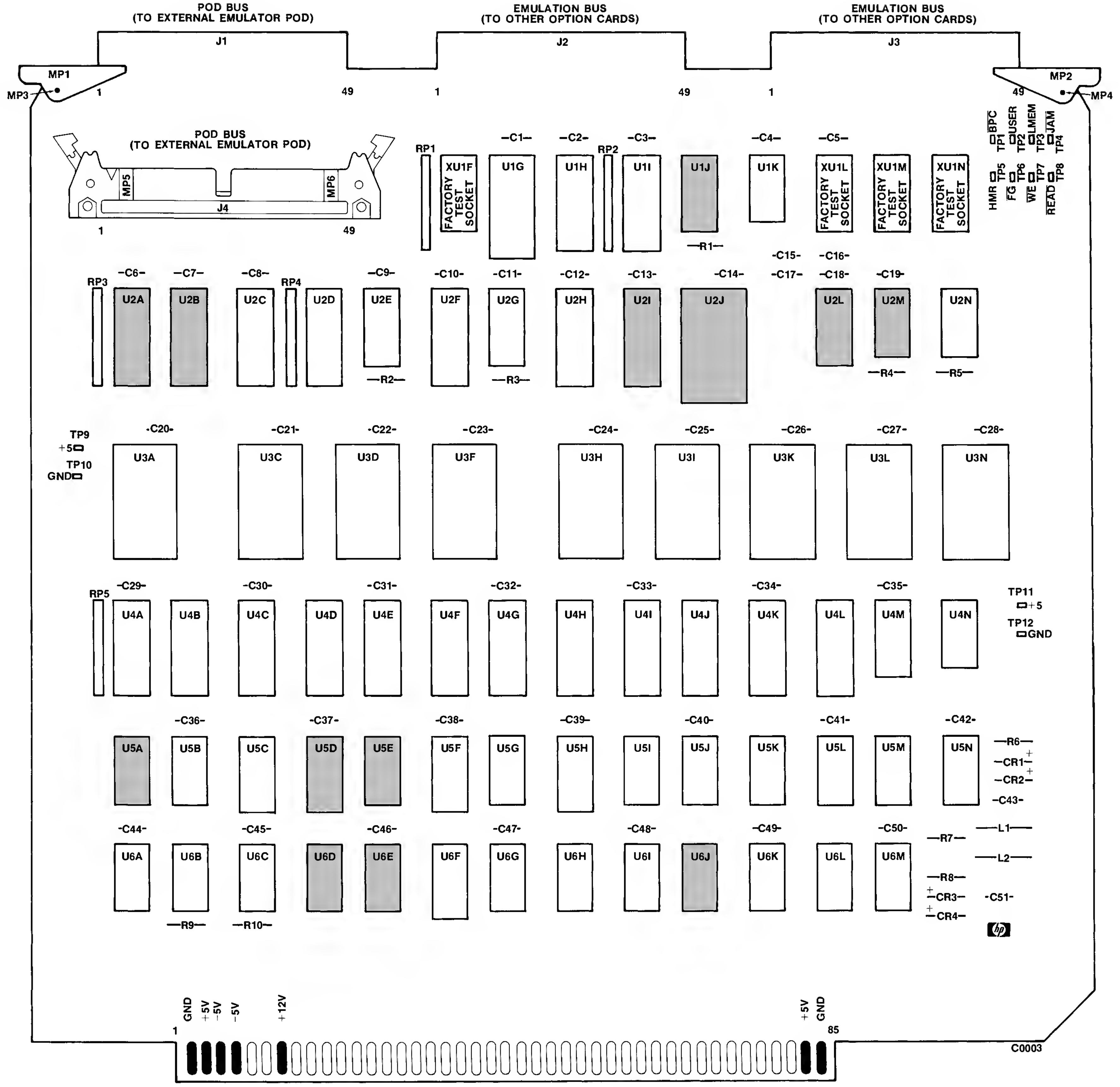
ICs On This Schematic

REF. DES	HP PART NUMBER	MFG. PART NUMBER	+5V PIN	GND PIN
U4M	1820-1430	SN74LS161AN	16	8
U5G	1820-1144	SN74LS02N	14	7
U5H	1820-1282	SN74LS109AN	16	8
U5M	1820-1199	SN74LS04N	14	7
U6D	1820-1197	SN74LS00N	14	7
U6E	1820-1112	SN74LS74AN	14	7
U6F	1820-1282	SN74LS109AN	16	8
U6G	1820-1197	SN74LS00N	14	7
U6H	1820-1144	SN74LS02N	14	7
U6I	1820-1202	SN74LS10N	14	7

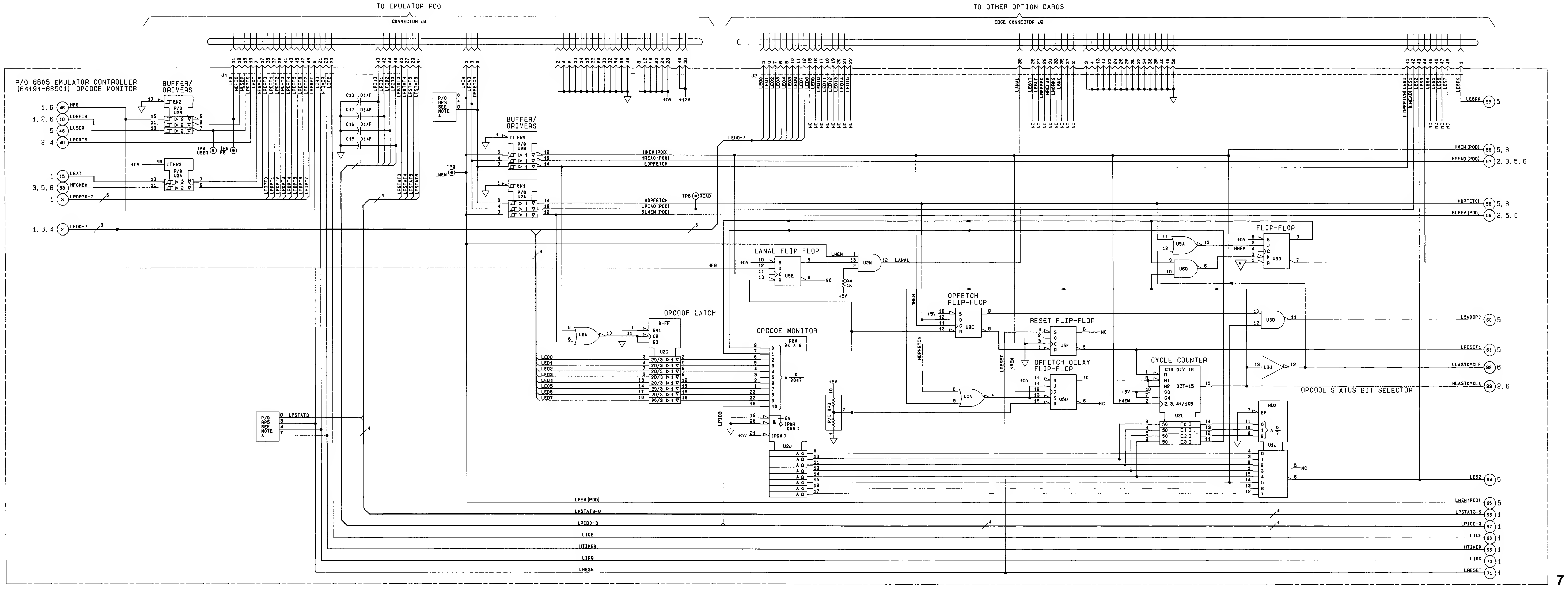
Parts On This Schematic

RP3.

Figure 8-9. Schematic 6
Foreground/Background Logic



Component Locator



ICs On This Schematic

REF. DES	HP PART NUMBER	MFG. PART NUMBER	+5V PIN	GND PIN
U1J	1820-1217	SN74LS151N	16	8
U2A	1820-1624	SN74S241N	20	10
U2B	1820-1633	SN74S240N	20	10
U2I	1820-2102	SN74LS373N	20	10
U2J	64191-80000	64191-80000	24	12
U2L	1820-1430	SN74LS161AN	16	8
U2M	1820-0686	SN74S11N	14	7
U5A	1820-1144	SN74LS02N	14	7
U5D	1820-1282	SN74LS109AN	16	8
U5E	1820-1112	SN74LS74AN	14	7
U6D	1820-1197	SN74LS00N	14	7
U6E	1820-1112	SN74LS74AN	14	7
U6J	1820-1199	SN74LS04N	14	7

Parts On This Schematic

C13,15,16,17. R4. RP3,4,5.

NOTE A

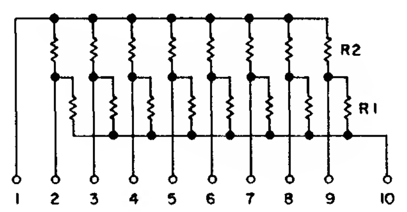


Figure 8-10. Schematic 7
Pod Interface and Opcode Monitor

Product Line Sales/Support Key

Key Product Line
A Analytical
CM Components
C Computer Systems Sales only
CH Computer Systems Hardware Sales and Services
CS Computer Systems Software Sales and Services
E Electronic Instruments & Measurement Systems
M Medical Products
MP Medical Products Primary SRO
MS Medical Products Secondary SRO
P Personal Computation Products
* Sales only for specific product line
** Support only for specific product line

IMPORTANT: These symbols designate general product line capability. They do not insure sales or support availability for all products within a line, at all locations. Contact your local sales office for information regarding locations where HP support is available for specific products.

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M

MOROCCO
Dolbeau
81 rue Karatchi
CASABLANCA
Tel: 3041-82, 3068-38
Telex: 23051, 22822
E

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Boite Postale 156
CASABLANCA
Tel: 272093, 272095
Telex: 23 739
P

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Hewlett-Packard Nederland B.V.
Van Heuven Goedhartlaan 121
NL 1181KK **AMSTELVEEN**
P.O. Box 667
NL1180 AR **AMSTELVEEN**
Tel: (020) 47-20-21
Telex: 13 216 HEPA NL
A,CH,CM,CS,E,MP,P

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Bongerd 2
NL 2906VK **CAPELLE, A/D IJSSEL**
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NL 2900AA **CAPELLE, A/D IJSSEL**
Tel: (10) 51-64-44
Telex: 21261 HEPAC NL
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Cable: HEWPACK Auckland
CH,CM,E,P*

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Courtenay Place, **WELLINGTON 3**
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CH,CM,E,P

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AUCKLAND
Tel: 794-091
Telex: 60605
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Northrop Instruments & Systems Ltd.
110 Mandeville St.
P.O. Box 8388
CHRISTCHURCH
Tel: 486-928
Telex: 4203
A,M

Northrop Instruments & Systems Ltd.
Sturdee House
85-87 Ghuznee Street
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WELLINGTON
Tel: 850-091
Telex: NZ 3380
A,M

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See United Kingdom

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Hewlett-Packard Norge A/S
Folke Bernadottes vei 50
P.O. Box 3558
N-5033 **FYLLINGSDALEN** (Bergen)
Tel: (05) 16-55-40
Telex: 16621 hpnas n
CH,CS,E,MS

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Österndalen 18
P.O. Box 34
N-1345 **ÖSTERÅS**
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OMAN
Khimjil Ramdas
P.O. Box 19
MUSCAT
Tel: 722225, 745601
Telex: 3289 BROKER MB MUSCAT
P

Suhail & Saud Bahwan
P.O.Box 169
MUSCAT
Tel: 734 201-3
Telex: 3274 BAHWAN MB

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Mushko & Company Ltd.
1-B, Street 43
Sector F-8/1
ISLAMABAD
Tel: 26875
Cable: FEMUS Rawalpindi
A,E,M

Mushko & Company Ltd.
Oosman Chambers
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***KARACHI** 0302*
Tel: 524131, 524132
Telex: 2894 MUSKO PK
Cable: COOPERATOR Karachi
*A,E,M,P**

PANAMA
Electrónico Balboa, S.A.
Calle Samuel Lewis, Ed. Alfa
Apartado 4929
PANAMA 5
Tel: 64-2700
Telex: 3483 ELECTRON PG
A,CM,E,M,P

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Arranged alphabetically by country

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Los Flamencos 145, San Isidro
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***LIMA** 1*
Tel: 41-4325, 41-3703
Telex: Pub. Booth 25306
CM,E,M,P

PHILIPPINES
The Online Advanced Systems Corporation
Rico House, Amorsolo Cor. Herrera Street
Legaspi Village, Makati
P.O. 8ox 1510
*Metro **MANILA***
Tel: 85-35-81, 85-34-91, 85-32-21
Telex: 3274 ONLINE
A,CH,CS,E,M

Electronic Specialists and Proponents Inc.
690-8 Epilanio de los Santos Avenue
*Cubao, **QUEZON CITY***
P.O. Box 2649 Manila
Tel: 98-96-81, 98-96-82, 98-96-83
Telex: 40018, 42000 ITT GLOBE MACKAY 8OOTH
P

PORTUGAL
Mundinter
Intercambio Mundial de Comércio S.A.R.L.
P.O. Box 2761
Avenida Antonio Augusto de Aguiar 138
P-LISBON
Tel: (19) 53-21-31, 53-21-37
Telex: 16691 munter p
M

Soquimica
Av. da Liberdade, 220-2
*1298 **LISBOA** Codex*
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Telex: 13316 SABASA
P

Telectra-Empresa Técnica de Equipmentos Eléctricos S.A.R.L.
Rua Rodrigo da Fonseca 103
P.O. Box 2531
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Telex: 12598
CH,CS,E,P

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A,CH,CS

QATAR
Computearbia
P.O. Box 2750
DOHA
Tel: 883555
Telex: 4806 CHPARB
P

Eastern Technical Services
P.O.Box 4747
DOHA
Tel: 329 993
Telex: 4156 EASTEC DH

Nasser Trading & Contracting
P.O.Box 1563
DOHA
Tel: 22170, 23539
Telex: 4439 NASSER OH
M

SAUDI ARABIA
Modem Electronic Establishment
Hewlett-Packard Olvision
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Thuobah
AL-KHOBAR
Tel: 864-46 78
Telex: 671 106 HPMEEK SJ
Cable: ELECTA AL-KHOBAR
CH,CS,E,M,P

Modem Electronic Establishment
Hewlett-Packard Olvision
P.O. 8ox 1228
Redec Plaza, 6th Floor
JEDDAH
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Telex: 4027 12 FARNAS SJ
Cable: ELECTA JEOOAH
CH,CS,E,M,P

Modern Electronic Establishment
Hewlett-Packard Olvision
P.O.8ox 2728
RIYADH
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Telex: 202049 MEERYD SJ
CH,CS,E,M,P

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CM

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A,CH,CM,E,MS,P

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CH,CS,M

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A,CS,MS,P

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Hewlett-Packard (Schweiz) AG
Allmend 2
CH-8967 **WIDEN**
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Cable: ELECTROBOR OAMASCUS
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Middle East Electronics
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M,P

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A

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Telex: 84439 Simonco TH
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Telex: 87669-8EQUIPT TH
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CM,E,M,P

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TUNIS
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Corema
1 ter. Av. de Carthage
TUNIS
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M

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Teknim Company Ltd.
Iran Caddesi No. 7
*Kavaklidere, **ANKARA***
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E

E.M.A.
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SHARJAH
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